# STATUS OF THE NSLS-II LLRF SYSTEM*

C. Marques†, J. Rose, N. Towne, B. Holub, F. Gao, G. Wang
NSLS-II, BNL, Upton, NY 11973, U.S.A

*Abstract*

The NSLS-II RF system uses an in-house FPGA based low level RF (LLRF) solution called the Cavity Field Controller (CFC). The CFC directs the amplitude and phase for the high power RF and directly influences beam acceleration and stability. In this paper we discuss a logically embedded network analyzer in situ with the digital feedback loop controlled via a MATLAB or EPICS interface. The embedded NA was used to evaluate the RF feedback stability and influence of the feedback parameters on the beam. We will also discuss diagnostics tools to investigate longitudinal beam dynamics and other functionality embedded into the FPGA fabric. Future development of the CFC implementation and hardware upgrades will also be discussed.

## INTRODUCTION

The Field Programmable Gate Array (FPGA) based CFC was developed as a common hardware platform for all NSLS-II RF systems. The reconfigurable logic on the FPGA allows the CFC to run in multiple modes of operation. For example, open loop feedforward (FF), closed loop feedback (FB) and a combination of the two. In addition to operating modes the CFC is able to run diagnostics, cavity tuner loop adjustments, data buffering, event handling including interlocks and real-time data acquisition simultaneously. The CFC includes eight 500 MHz RF inputs and one 500 MHz RF output along with multiple IO which can be seen in Figure 1. More information about the digital controller can be found elsewhere [1].

## CFC FUNCTIONS

One of the primary functions of the CFC is a feedback control loop of the cavity field. A simplified schematic of the feedback loop and other CFC logic can be seen in Figure 2. The feedback loop includes digitized vector signal detection provided by dual 14-Bit ADC LTC2299s at 80 MHz (40 MHz/channel) and can be seen in the schematic by the $I, Q, -I, -Q$ sequence just after the cavity pickup. The $I, Q, -I, -Q$ notation comes from the fact that the 50 MHz IF is sampled at half the clock frequency or 40 MHz. The digitized sequence is then corrected for feedback path latency of approximately 1.1 ms using a phase rotation provided by the $Kp(I)$, $Kp(Q)$ multipliers and where the total $Kp$ magnitude is $|Kp| = \sqrt{Kp(I)^2 + Kp(Q)^2}$. Digital signal processing using a host-front end is used to calculate and properly adjust the loop phase rotation. The summed $I$ and

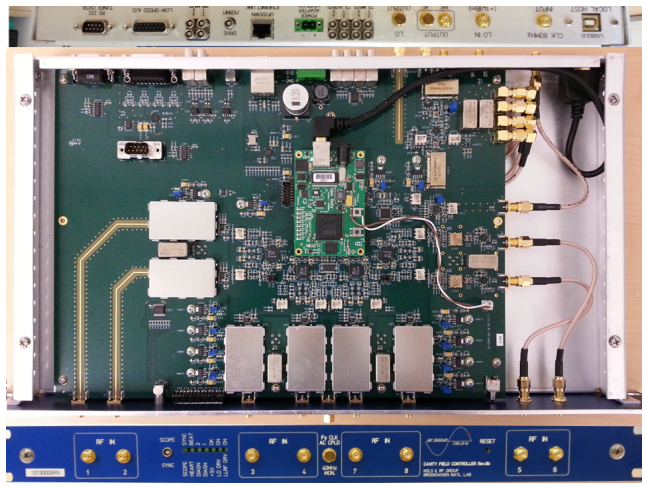

Figure 1: Picture of the CFC. The top and bottom of the picture shows the different IO on the back and front panels respectively.

$Q$ pair is multiplied by the integral gain factor $Ki$ and subsequently summed. It is worth noting that the integral gain $Ki$ is dependent on the proportional gain $Kp$ and hence so is the corner frequency or bandwidth of the feedback loop. The summed error signal produced in the integral leg of the feedback loop not only provides for error correction but also synthesizes the output drive signal for the CFC.

### *Network Analyzer*

The logically embedded vector network analyzer produces a direct digital synthesized (DDS) stimulus which is summed with the output drive of the controller. The network analyzer module performs a fourier analysis on the CFC readbacks to produce response functions of those readbacks normalized to the DDS output. Much like an $S_{21}$ measurement on a conventional network analyzer except in this case we have several inputs including the feedback loop and longitudinal beam motion from a summed beam position monitor (BPM). Using a narrow bandpass filter of 540 kHz with a center frequency of 499.68 MHz, we eliminate any problematic signals including the charge induced by an empty bunch train from the storage ring fill pattern and we are able to measure a unambiguous beam response. Figure 3 shows the amplitude response function of the cavity field and BPM. The figure shows that for a fixed integral gain $Ki$ and DDS amplitude, the proportional gain $Kp$ influences both the beam and cavity response to the stimulus. For higher $Kp$ gain the effect of the beam from perturbations is decreased and suggests higher stability and lifetime. This effect is also shown by the narrowing of the peak at the synchrotron frequency for increasing $Kp$ values. Figure 3 also shows

* Work supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-SC0012704.
† cmarques@bnl.gov

ISBN 978-3-95450-189-2

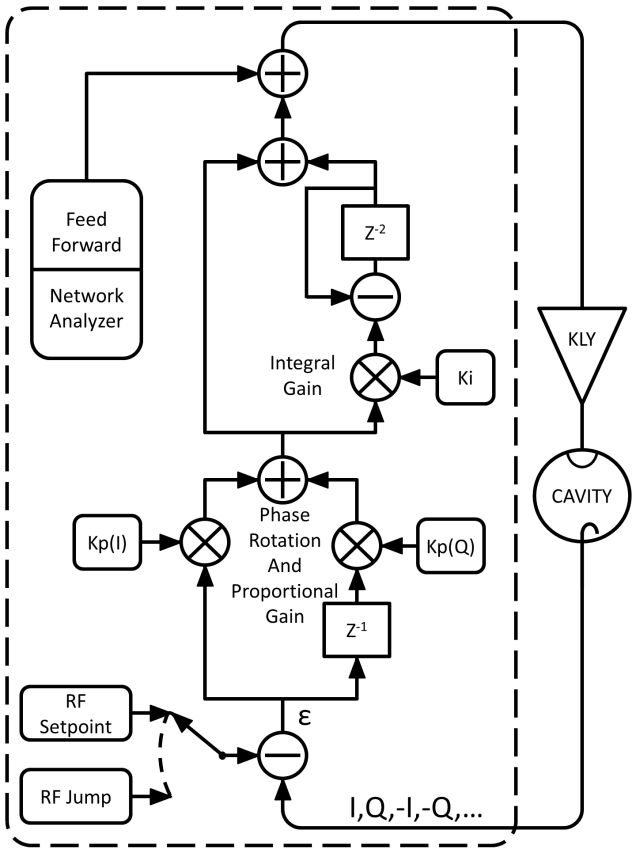


Figure 2: Simplified schematic of the CFC logic and feedback loop.

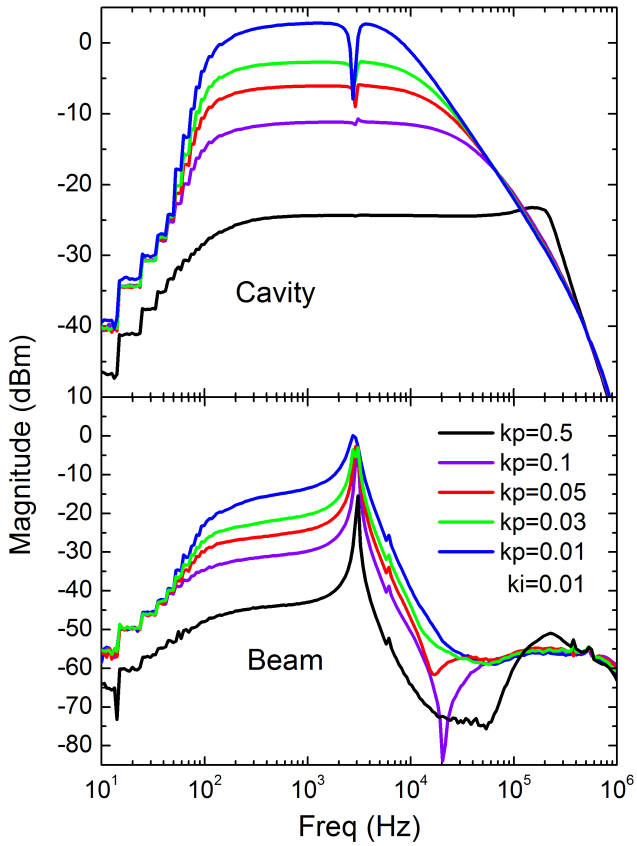


Figure 3: Cavity and beam frequency response. For the above plots there are two cavities 1.2 MV each and 150 mA beam current in the ring. Integral gain is constant at 0.01, proportional gains are 0.01, 0.03, 0.05, 0.1 and 0.5 respectively.

typical bandwidth extension of the cavity field for increasing $Kp$ at the expense of the amplifier gain.

### *Circular Buffer*

The circular buffer module in the FPGA code continuously writes streaming data from the CFC inputs to the on-board RAM in a cyclic fashion. In the event of a circular buffer trigger the data stream continues to be written into the RAM approximately half of the memory capacity. Since there is an $I, Q, -I, -Q$ data stream at 40 MHz, at least two data points to establish amplitude and phase. Currently we continuously monitor five channels which yields time resolution of 250 ns. With 1703936 samples we can view ~213 ms of data before and after the trigger. This data can then be imported into a host computer and processed into a waveform.

### *Phase Jump*

The feedback loop error signal is generated by subtracting the cavity field input from the setpoint data stream. The phase jump module in the FPGA code allows switching of RF setpoints, more precisely the $I/Q$ set points and so can either be an amplitude and/or phase jump. A phase jump was used in beam studies where phase jumps of 100 degrees or more with beam were implemented. The limiting factors for the magnitude of the phase jump are the forward and reverse power limits of the RF system. These are in turn influenced by the size of the phase jump (180 degrees gives maximum power requirement) and the time to complete the jump. This time depends in turn on the feedback gain set points. When the phase jump is triggered the set points immediately change to new values. The cavity field fed into the controller is subtracted from this set point and the error is multiplied by the feedback gains to drive the system to the new values. An example phase jump can be seen in Figure 4 where the cavity field phase was altered by more than 100 degrees causing the beam phase to also readjust by more than 100 degrees. The RF phase jump can induce longitudinal beam oscillations which can be seen in the inset of Figure 4 and serves as a powerful tool for investigating longitudinal beam dynamics.

Using this module and turn-by-turn BPM data several experiments were carried out, i.e. measured the NSLS-II ring momentum aperture with and without damping wigglers, we located the momentum aperture limitation and initiated beam crossing major resonance under the stopband width control [2].



ISBN 978-3-95450-189-2

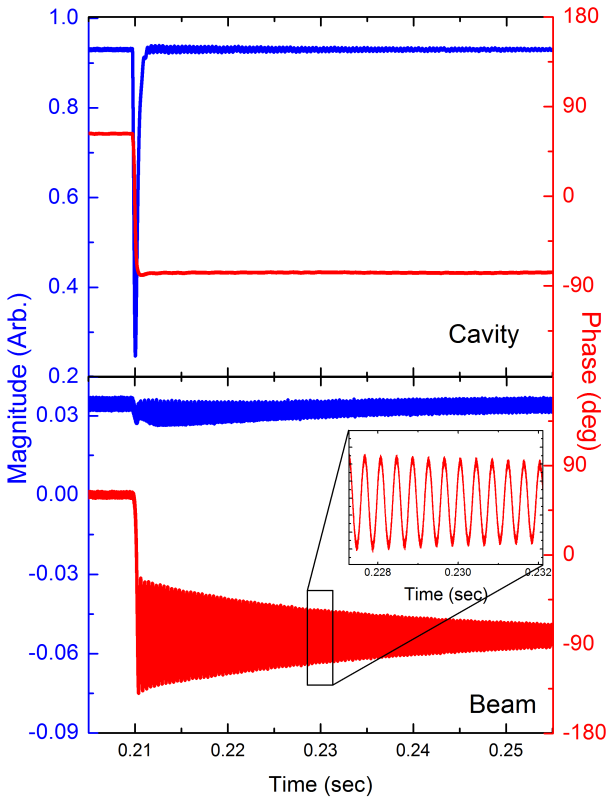


Figure 4: Circular buffer data of a phase jump experiment. The blue and red traces represent amplitude and phase respectively.

### *Pulsed Gains*

The feedback control loop discussed above uses programmable feedback gain settings. An NSLS-II RF system model suggests that system stability might be achieved with gain settings that are a factor 100 higher than are currently in use. The high gains would also make them hard to find if the tolerance about such settings is small, or if there is no stable path between current settings and the higher ones. Such values would be highly advantageous not only because of the quick damping of synchrotron oscillations, but also for greater suppression of noise in the system at other frequencies, such as power-supply noise. The pulsed gains module allows the logic to switch repetitively to alternate gain settings at various timescales while the user watches a scope trace for instabilities. When stable settings are found, those settings are fine tuned and the switched time is progressively increased to verify stability. When running repetitively at a rate of once or twice a second, the gain/phase parameter space should be quickly found, even areas far removed from current settings.

This technique is used in other contexts, such as when pulsing coupled-bunch feedback off to measure growth rates of individual modes, when switching between cavity-phase setpoints as a means to study longitudinal dynamic behavior described above, and the analogous technique of pulsing feed forward when tuning feedback.

## DEVELOPMENT

Although the CFC is highly versatile and expandable there is still room for improvement. One such improvement is converting to a FPGA System on Chip (SoC) device which integrates the programmable software of a processor with the programmable hardware of an FPGA. Software programmability should include supporting an operating system such as Linux or comparable to handle many functions for the FPGA. These functions include communications protocols, filesystems, DSP, peripheral device handling and any host operation described above provided the right drivers and appropriate hardware is installed. The 32 MB system RAM on the CFC is also a bottle neck and must be upgraded to support larger feedforward/feedback ramp tables and potentially longer circular buffer data. High speed transceiver capabilities are also a possibility for inter CFC communications and system diagnostics which would also free up some of the IO on the CFC. NSLS-II uses event generators (VME-EVRRF-230, PMC-EVR-230, etc.) to create a timing system [3]. Currently the CFC does not support event receivers (EVRs) and so having EVR capabilities would eliminate timing jitter, improve beam studies and overall CFC functionality.

## SUMMARY

An FPGA based CFC is being used successfully in the NSLS-II RF systems. The flexibility of the FPGA allows for developing powerful tools embedded in logic. Tools including a vector network analyzer, circular buffer, phase jump and pulsed gains were used to further understand and improve the RF systems. Further development of the CFC is ongoing.

## ACKNOWLEDGMENT

The authors wish to acknowledge the help and discussions of Jueri Tagger and Ruslan Kadyrov. In addition the continuous support from the NSLS-II Controls and Utilities groups.

## REFERENCES

[1] B. Holub *et al.*, "NSLS-II Digital RF Controller Logic and Applications", in *Proc. IPAC'15*, paper MOPTY038.

[2] G. Wang *et al.*, "RF Pinger Commissioning and Beam Dynamics Studies at NSLS-II", in *Proc. IPAC'16*, paper THOBA01.

[3] M. Davidsaver, "EVR Usage Guide", BNL Controls Internal Document, August, 2015 Rev. 7, `https://wiki.bnl.gov/nsls2controls/index.php/Timingref`



ISBN 978-3-95450-189-2