HARMONY: A GENERIC FPGA BASED SOLUTION FOR FLEXIBLE FEEDBACK SYSTEMS

X. Serra-Gallifa†, J. Avila-Abellan, M. Broseta, G. Cuni, D. Fernandez-Carreiras, O. Matilla, A. Ruz, ALBA-CELLS Synchrotron, Barcelona, Spain

Abstract

Feedback and complex acquisition systems usually need real-time interaction among instruments with microsecond's time response. These implementations are hard to achieve with processors but feasible using FPGAs. There are some cases, such as synchrotron beamlines, where high flexibility and continuous tuning are also required, but the implementation of multiple full-custom FPGA designs are extremely time-consuming. Harmony is a solution based in FPGA that offers, via high level programming, a unique framework with common time base, data acquisition, storage, real-time processing, data sharing and diagnostic services designed to implement flexible feedback systems. It is based in two interconnected buses: Self-Describing Bus, developed at CERN/GSI under OHWR license, that communicates with Control System; and Harmony Bus which creates a bus framework where different modules can share timestamped data capable of pre-programed events generation. The first version of Harmony is already successfully being used in Em# project which objective is the development of a performant four-channel electrometer.

ELECTROMETER'S DEVELOPMENTS AT ALBA

During the phase design of the beamlines of ALBA the large number of four channel electrometer needs lead Computing Division to the development of a medium performance electrometer oriented to diagnostic applications [1]. The simplicity of integration in the beamline Control System was one of its main goals. The project was a success with more than 40 units installed and a very good performance of the current amplifier. Inherent analog capabilities extended the use of the electrometer to more complex requirements. Soon it was agreed that a new development project to take advantage of the current amplifier performance was needed to improve different aspects [2, 3]. The main points focused on:

- Improving the signal to noise rate increasing the digital resolution up to 18 bits and the sampling rate.
- The possibility to perform current measurements under voltage biased conditions up to 1 kV and also to avoid ground loops.
- Capability of implementing real-time feedback systems.
- Minimizing the obsolescence problems by adopting a flexible and modular architecture based in standards.

HARMONY: A FLEXIBLE FEEDBACK SOLUTION

From the beginning of the project, it was clearly seen that the new electrometer (Em#) should be easily adaptable to future needs of beamlines experimental stations. However, there is always a trade-off between performance and flexibility. Since the Em# is mainly designed to fulfil the requirements of the Beamlines in a Synchrotron (although is applicable in many other environments) a detailed analysis of the latencies needed by the different "players" was carried out. It states that:

- Low current measurements (bellow µA) have inherently due to its high gain stages and parasitic capacitors maximum bandwidths of few kHz.
- Encoder or trigger readouts can reach frequencies of few MHz.
- Actuators and motor reaction times are higher than hundreds of microseconds.
- Data acquisition timestamped in the microsecond range enables the correlation of different instruments' data during the analysis.

Therefore the solution targeted feed-back systems at frequencies up to 10 kHz, and consequently the FPGA technology was chosen among different options including several microprocessors.

Actually, the performance of modern FPGAs is largely sufficient for the required feedback speeds, with clock frequencies allowing hundreds of clock cycles to process inputs and produce outputs. This enabled a FPGA architecture with independent blocks sharing data. It was also considered that the use of a bus for data sharing design would optimize the desired flexibility for multiple applications.

Development in Workgroup

In previous developments at ALBA, the electronics engineers developed the hardware, gateware (FPGA software) and firmware; once everything was tested it was delivered to software engineers who integrate the instrument in the control and data acquisition system and developed the user interface. In order to overcome this issue, this new project incorporated the contributions from the software engineers earlier in the schedule, reducing the number of late requirements to the hardware and working in parallel shortening the whole duration of the project.

This approach involved a clear definition of the project and its interfaces from beginning. A crucial help to

† xserra@cells.es

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achieve this objective was the use of Self-Describing Bus (SDB) [4] available in Open Hardware (OHWR). SDB defines a protocol of communication that enumerates all the cores of the hardware in a tree-like structure, similar to a filesystem with folders (see Figure 1). The OHWR community has made available a number of tools of great value to this project such as wgen2 [5], which generates a memory map of the whole set of registers in C and VHDL from a text configuration file specification of the core. This tool defined a "de facto" interface for hardware and software and consequently fostered the development in parallel. The modifications appeared during the development of the project were orchestrated as formal reviewed improvements of this interface. Also the granularity of the project in well-defined cores accessible from high level software allows a segmentation of the functionality of the device and makes simpler the development and tests of the software.

Origin of Harmony

The flexibility given by the SBD had some disadvantages: the communication between the cores was not flexible and fast enough for the needs of the project. The intercommunication between cores using the SDB showed latencies way above the requirements and was not deterministic.

The Harmony Bus (HB) was the proposed solution for a fast interconnection between cores overcoming the aforementioned limitations. The HB will act as a second optional bus for fast data sharing between cores, following the structure of SDB.

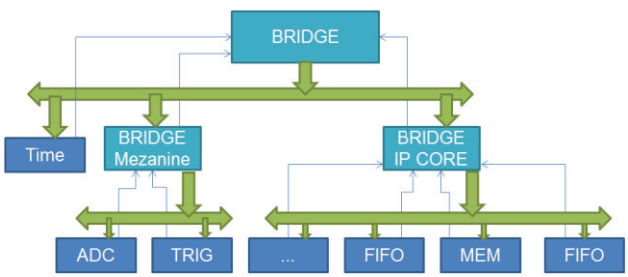

Figure 1: Data flow of the Harmony Bus physicaly implemented as a tree structure. The thin arrows represent the upstream bus and the green thick arrows represent the broadcast bus.

Harmony in Detail

One of the main components of HB is the set of Harmony Bridges, following the nomenclature of SDB. The cores are connected to bridges by HB, which act as bus arbiters. The cores send their data to a Harmony bridge, which gateway the frames to the top layer all the way up to the top Bridge (see Figure 1). Finally the top bridge broadcasts the data back to all components through the set of bridges, which register the broadcasted data to fit easily the timing constraints.The bridges add latency and jitter to the messages, but still the bus is fast enough (125 MHz) so these delays became negligible and the system is perceived as an instantaneous pool where all components share their data among them (see Figure 2).

The HB is composed of 2 buses one for sending messages and a second where bridges broadcast all messages received. Both are 64-bit buses composed by 32 bits for data, 24 bits for timestamp in nanoseconds (TS) and 8 bits dedicated to data source identification (ID). There are also 3 lines for bus handshaking, one line indicating valid data in broadcast bus and 2 lines (data request and reading) to manage the upstream bus (see Figure 4).

The data transmitted by HB have an ID of 8 bits which allows up to 256 different sources. The IDs are assigned to each component by the control software via the SDB. There are two reserved message IDs: ID 0 is used to reset TS every 16 ms acting as a periodic time reference, and ID 255 is reserved for error messages.

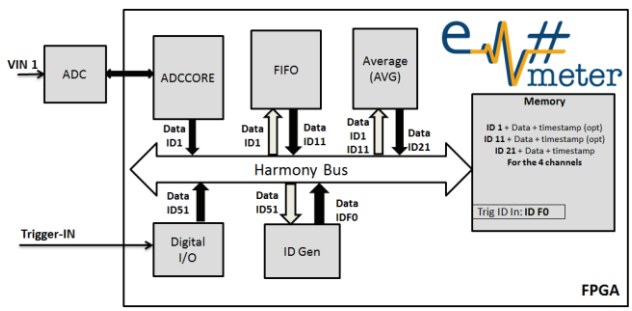

Figure 2: Block diagram of Em# Harmony implementation.

The Harmony bridges do a continuous diagnosis of the HB, measuring parameters like data sent or the maximum number of occupied slots. These parameters are accessible via SDB and allow the high level software, for example the control system to check the HB occupancy. Also each core has status flags used to ensure a correct communication process.

EM#. NEW HARDWARE MORE THAN AN ELECTROMETER

In addition to the SDB bus, other major decision was was the FPGA board (SPEC) developed at CERN in OHWR. The use of that FPGA board speeded up the development, as some critical issues were already tested for the OHWR community.

Em# included a Single board computer (SBC), running a Linux based operating system where the software for managing the configuration, data transfer and communication with the outside world is executed [6]. The SBC performs communications with the outside wolrd via a 1 Gb Ethernet link, and also manages different diagnostics such as monitoring the temperatures and the consumption of different parts and communications using 1xPCIe port to FPGA.

The Em# also features custom electronics designed at ALBA such as a ADC FMC board, a Front Panel Board, a Current Amplifier Carrier Board, 4 Current Amplifiers Boards and a Power Supply Board. That hardware includes an 18-bit ADC isolated up to 1200 V, that reads

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4 current amplifiers with 7 ranges from 1 mA to 100 pA, also isolated. Furthermore, the front panel has 4 analogic outputs, 4 digital In/Out Coaxial ports that support up to 100 MHz, and 9 In/Out differential ports (RS422) that can be used for synchronization or feedback implementations (Figure 3).

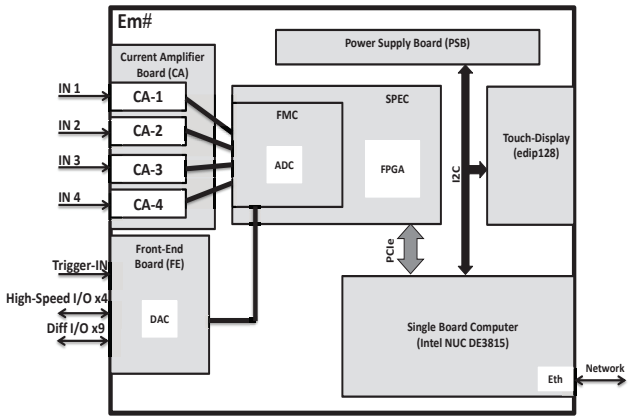

Figure 3: Em# hardware block diagram.

Harmony in Em#

The HDL cores already implemented in the FPGA are:

- ADCCORE: Component that controls the ADC device using high-speed serial lines.
- FIFO: used for storage or delays any data from a pre-specified ID. There is one module per channel.
- AVERAGE: used to calculate a dynamic average of data in 32-bit 2-Complement format. There is also one module per channel.
- ID GEN: generates data with and ID. It can be used to setup memories or for diagnostics
- Memory: Ram memory used to store data from fast BUS. It implements a circular buffer that can be started/stopped from fast or slow bus
- Digital I/O: Controls the digital input output ports. It can be used to implement a counter or an external trigger.

A typical example of an acquisition using the Harmony Bus is shown in Figure 2: the data acquired by the ADC in channel 1, is read by the ADCCORE block and sent to the Harmony bus with the identifier ID1, to be processed by the other modules, if necessary. FIFO uses the data with ID1 and generates a frame sent to the Harmony Bus with ID11 (containing data from the ADC delayed some messages). Average block sums data with ID1 and subtracts data ID11 from an accumulator register and generates data ID21. All the data sent to the Harmony Bus is available to be stored in memory block. Before starting the acquisition, at configuration time, the main software in the SBC setups how every component should behave in the HB. These communications between cores can be seen in the screenshot of Figure 4.

CURRENT STATE

After the first production tests, the first production of the Em# has already been launched. The project has enlarged the scope since one year ago when MaxIV and ALBA decided to create a international collaboration to further develop Em# architecture. A functional prototype is already working and 12 units are being produced by ALBA and 50 units by MAXIV. The Em# will be in both facilities the standard electrometer to be used for new installations. The first units are expected in mid-November.

From the technical point of view the future developments will be focus in the implementation of the management of the SPECS DDR3 memory and the DMA access from SBC to FPGA.

Moreover one the future challenges already considered in Em# architecture is to share the deterministic network provided by the Harmony among different Em# units to extend for example the feedback capabilities. One of the upcoming hardware developments for the platform is a multiple Input/Output module. Most of the components for such a module are already in place.

Finally a math processor for real-time calculus in the FPGA is also foreseen. This will increase the feedback capabilities of the Harmony devices.

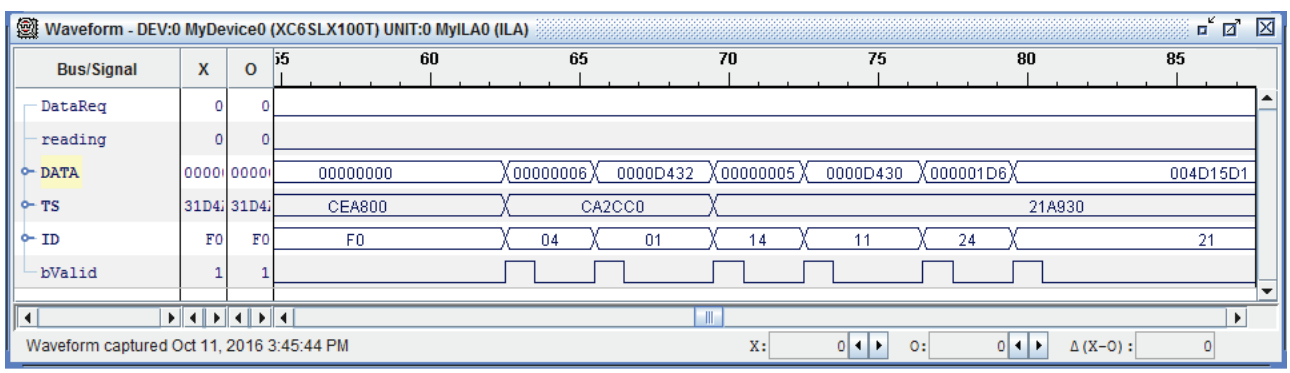

Figure 4: Data trace from ChipScope application, where it is shown the 3 control lines and the broadcast bus in a real Em# acquisition. ID0F is the trigger from the Digital IO block, ID04 and ID01 are the outputs of channels 1 and 4 of the ADC, ID14 and ID11 are the FIFO messages and ID21 and ID24 are the outputs of AVG Blocks.

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CONCLUSION

The development of Harmony is finished and the first units are being manufactured. The design overcomes the problems identified in the first version and fulfils the requested project specifications being flexible, scalable and easy-to-upgrade. The modularity of the project naturally fosters several developers working on different parts of the project simultaneously. Few months ago, MAXIV and ALBA signed a collaboration agreement, also open to other institutes to join, to further develop the system in a continual improvement lifecycle.

Harmony will be the development framework for new instrumentation designed at ALBA, profiting of the flexibility of the platform, maximizing the possibility of interconnection of devices and sharing a common timebase for precise timestamps of data.

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