OPEN HARDWARE EXPERIENCE ON LNLS' BEAM DIAGNOSTICS

G. B. M. Bruno*, D. O. Tavares, H. A. Silva, F. C. Sant'Anna,
J. L. Brito Neto, L. M. Russo, L. A. Martins, S. R. Marques
LNLS, Campinas, Brazil

Abstract

LNLS Beam Diagnostics Group has decided to adopt and develop open-hardware technologies for most of its projects, partnering with other institutes and companies to design and build a complete RF BPM electronics, from the BPM pick-up to the operator interface. That decision resulted in advancements and learning, bringing new technologies, flexibility and knowledge, but also brought some hardships and new challenges. This paper details the history, advantages and difficulties of this open hardware approach.

INTRODUCTION

Sirius is the new synchrotron light source currently being built by LNLS in Brazil, with 518.4 m circumference and expected to be installed in late 2017, for commissioning in mid 2018 [1]. A total of 255 units of in-house-developed BPM electronics will be built in order provide feature-rich data acquisition system for button and stripline BPM pick-ups of the storage ring, booster and booster to storage ring transfer line.

The Sirius digital BPM electronics consists of 4 main pieces of hardware: a standalone RF front-end electronics for analog signal conditioning (RFFE), a digitizer mezzanine card for analog-to-digital conversion (FMC ADC), a FPGA-based carrier board acting as a digital back-end for acquisition, signal processing and communication (AMC FMC Carrier - AFC), as depicted in Fig. 1 and a COTS MicroTCA.4 crate providing a wealth of services for the digital back-end and its mezzanine cards, including power supply, cooling, crate management, a CPU host and shared trigger and clock lines for all crate slots. The crate hosts several digital back-end boards (up to 10), whereas each digital back-end board hosts 2 digitizer mezzanine cards. Each digitizer has 4 ADC channels thus being able to digitize the set of 4 analog signals provided by each BPM pick-up.

Apart from the COTS crate and its infrastrucutre components, all electronics developed by LNLS for the Sirius RF BPM electronics are open hardware, licensed under the CERN OHL license [2] and available through the CERN Open Hardware Repository [3]. The following sections will give a brief motivation for the adoption of open hardware, in general and in the context of Sirius electronics development, and then will describe the evolution of three open hardware projects: RFFE, FMC ADC and AFC.

THE OPEN HARDWARE APPROACH

There are several different definitions and intents associated with the names "open hardware" and "open source hardware", which are, sometimes, conflicting ones. The most common meaning, borrowed from the free software and open source software initiatives, requires the user to have access to the design files, being allowed to do modifications, to distribute and to use the project without restrictions [4]. Public release of the work may be required by some definitions, such as the one defined by the Open Source Hardware Association (OSHWA) [5], while some licenses, such as CERN OHL [2] may only require documentation to be sent to users who acquire the products.

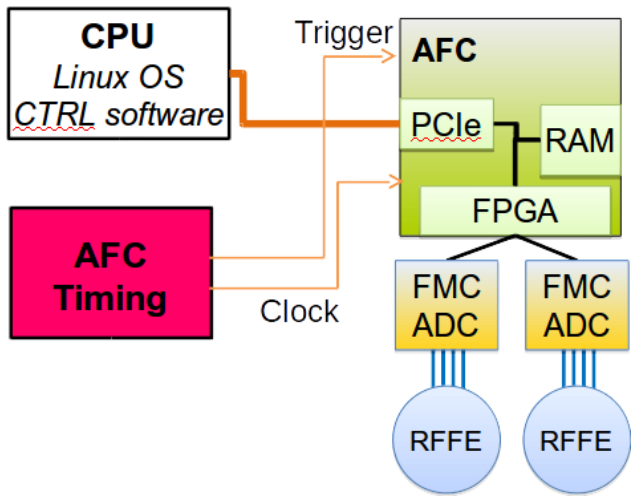

Figure 1: Simplified scheme for Sirius BPM electronics.

An important and frequently misunderstood aspect of the open hardware definition is its use in commercial applications. Most open hardware definitions do not prohibit commercial use of the project, in fact, most of them explicitly allow commercial use, indistinctively of application or profit intention. In effect, open hardware advocates usually do not consider restrictions on commercial use to be legitimate on open hardware projects [5, 6]. All definitions, licenses and projects discussed in this work allow for unrestricted commercial use.

The motivations for adopting open hardware often includes better collaboration among users and suppliers, reducing of work duplication on similar projects, and allowing for quick advance on technologies by improving existing designs. For science instrumentation, open hardware may be preferred as a mean to allow or facilitate experiment duplication and to fully document and submit the results to peer review. An open hardware adopter is also less dependent on a specific company, as several different companies may produce and support the same open hardware design, or variations of it.

* gustavo.bruno@lnls.br

ISBN 978-3-95450-189-2

Besides those advantages, the adoption of an Open Hardware License such as CERN OHL, with common and well known terms, assures users and commercial companies they have the legal rights to allow using, modifying, producing and selling the developed hardware without risk of facing legal sanctions.

In addition to this legal assurance, the CERN OHL license requires derivative works to also be licensed by the same terms. Thus, users who receive modified versions of CERN OHL-licensed designs are entitled the same rights defined by the license, such as receiving the design files and being allowed to distribute it. These obligations also apply to designers who use part of a licensed design on other projects.

These rights and obligations, along with the centralized repository, initiatives and tools, intend to encourage the community to share the knowledge, design files and to avoid an open project from becoming closed, contrarily to the original designer goals. They also give legal assurance to commercial entities, which may profit from them by selling implementation and granting support.

Open Hardware at LNLS

The LNLS Beam Diagnostics Group decided to adopt open hardware for its BPM system after the resolution of designing its own version of the electronics was made, in order to bring knowledge and experience to the LNLS team in the area, and also to improve our autonomy and facilitate upgrades and improvements to assist in building a high-performance light source.

In this context, and inspired by the Open Hardware Initiative created by CERN in 2011, we took the open hardware path in a desire to allow better coordination with other laboratories, to reduce design effort by making use of existing designs and to help future maintenance by sharing the design updates with other agents. The open-hardware approach also mean we would be less dependent on third parties in these and future projects.

The following sections look into the development path which has been taken for each of the projects of the Sirius RF BPM electronics development. Despite the seemingly uniform approach around open hardware, the projects evolved differently, presenting both unexpected difficulties and opportunities of this.

ELECTRONICS DEVELOPMENT

AMC FMC carrier

The AMC FMC Carrier, or simply AFC [7], is a fairly complex board of our BPM system, and also the most versatile. At Sirius' BPM electronics, it works as the digital back-end of the system, hosting the FMC digitizers, doing digital signal processing and communicating with the rest of the system.

The AFC, as shown in Fig. 2, is a double-width PICMG AMC compliant board, and able to make use of most of the AMC Ports. It can be extended via two FMC HPC connectors and one µRTM connector, all capable of receiving and transmitting clock, LVDS and high-speed digital signals. Internally, if features a Xilinx Artix-7 FPGA, a clock crossbar able to dynamically route clock signals between the FPGA and all the connectors, and also low-jitter clock generation capabilities, enabling the board to be a White Rabbit timing receiver. A LPC176x microcontroller is responsible for board management and IPMI functionality.

Figure 2: AFC v3.1 with FMC130 mounted.

The development began in 2011, through a partnership between LNLS and the Warsaw University of Technology (WUT). Initially thought to be based on a stand-alone 18-slot FMC carrier [8], also an open hardware project, in 2012 its specification was changed to a MicroTCA AMC board to allow for reuse of the project in other applications and to leverage the infrastructure of the MicroTCA system.

The conceptual design was originally created by LNLS and evolved through request of comments in public mailing list [9], while the actual schematics and layout of the board were done under contract with the WUT, which also manufactured the first version of prototypes. The original design reused many circuits and parts from other open hardware FMC carriers, for instance SVEC [10] and SPEC [11].

After this first version, other 2 versions and 2 minor revisions of the board were designed by several actors: WUT, Creotech Instruments SA, and, more recently, LNLS. The modifications in these versions added features, corrected bugs, improved manufacturability and updated components part numbers.

In addition to its primary use in the RF BPM system, there are at least two other planned uses at Sirius for the AFC: fast orbit feedback (FOFB) processor board, and timing receiver. The FOFB processor is basically a concentrator of scynhronized beam position data of the whole storage ring and a feedback controller processor and must make use of the several multigigabit interfaces of the AFC. The timing receiver takes advantage of an assembly variation that routes signals from the µRTM module to the FPGA tranceivers, allowing low-jitter clock recovery and precise event signaling. The precise clock reference may then be distributed to the crate controller (MCH), from which it may be routed to all other boards in the crate, while events can

ISBN 978-3-95450-189-2

be decoded by the AFC and converted to trigger signals in bused MLVDS lines on the MicroTCA.4 backplane.

A µRTM optical receiver board [12], also an open hardware project, was used for prototyping the system and improvements in both AFC and SFP µRTM are being made by LNLS to better suit our timing system.

The current AFC version is 3.1, with an update expected to later this year with minor improvements, updated part numbers and improved manufacturability to better suit Sirius' final production.

FMC Digitizer

The FMC digitizer, as the name implies, is a mezzanine board hosting the ADCs for RF signal digitization. It is designed for direct sampling of RF signals coming from a beam position monitor, using four high-speed ADCs able to accept frequencies around 500MHz. The board may also generate the ADC clock signals in free running mode or locked from an external reference, allowing coherence between sampling and accelerator's RF frequency.

For the initial development of the FMC digitizer, LNLS contacted and asked for quotes for a contract design from several companies. Prices from most companies that accepted doing the open source design were deemed too high by LNLS, although one accepted developing the open-source hardware as long as LNLS guaranteed acquisition of 200 boards beforehand. However, due to the uncertainty of the final number needed by Sirius and to the difficulty to determine the final price of the boards before the design starts, in-house design was preferred.

The board was then designed by LNLS beam diagnostics team in 2012 and then manufactured, with some modifications, by WUT. This process resulted in two versions of the FMC digitizer: FMC130 [13], which employs Linear Technologies' LTC2208 and was mostly designed by LNLS personnel, and FMC250 [14], which employs Intersil's ISLA216p25 and is mostly designed by WUT. Some design features, such as VCXO and PLL circuits, the front panel and heat sink, are shared between the boards, while the analog input and digital ADC interfaces are different between the boards.

The first board to be tested by LNLS was the FMC130, with satisfactory results [15]. These digitizers were used for most of the BPM electronics evaluation at LNLS until 2016, when we started evaluating a change to a ISLA216-based design. The main expectations are a reduced operating temperature and a slight improvement in SNR performance (2dB). LNLS team indicated that FMC250's analog input return loss and linearity underperformed when compared with FMC130's, and should be improved [16].

As both boards have a CERN-OHL license, design pieces from LNLS's FMC130 could be directly transported to the Creotech's FMC250 project, speeding up development.

RF Front End

The RF front-end is the analog conditioning module of the BPM electronics, composed of two RF boards and a digital controller board. The three boards are placed together in a mechanical enclosure as depicted in Fig. 3. To improve stability, the RF channels are switched in pairs, and the signal is them band-pass filtered around 500 MHz, and attenuated or amplified to make use of the most linear region of the ADC. The controller board houses power supplies and a microcontroller for setup and communication.

To enable collaboration with other accelerators, a decision was made to follow the open hardware approach of the rest of the BPM system. The design files for the RFFE, consisting in PCB files for the three electronics boards and CAD files for the mechanical parts are currently available at the OHWR, with a CERN OHL license.

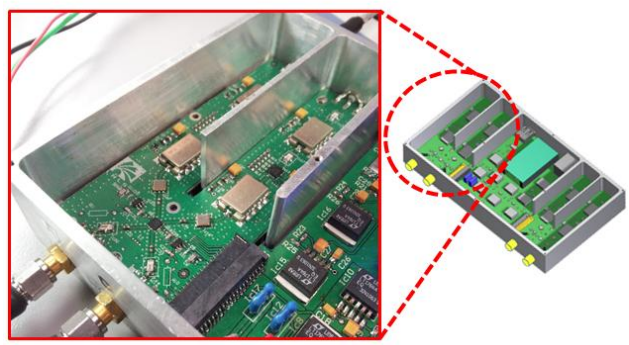

Figure 3: RFFE in its enclosure, RF channels A/C in detail.

SHORCUTS AND PITFALLS EXPERIENCED BY LNLS

The main advantages LNLS experienced from its open hardware experience were the quickier design time and fast evolution of the projects. The bigger disadvantages were the lack of good documentation and support, specially while developing supporting software, and the difficulties on manufacturing a complex board for the first time.

AFC

The AMC FMC Carrier profited the most, but also presented most pitfalls of all the three parts of the system. Open hardware has allowed white-rabbit support, even before LNLS had enough knowledge to make use of it, simply by taking the datasheet and layout from SVEC and SPEC.

While LNLS was focused on other developments and simply using the AFC, WUT and Creotech has gone forward with the project, adding features such as the µRTM connections and the making minor revisions to improve and update the board. This continuous update of the project by several agents is one advantage enable by open hardware.

Issues on software and firmware support were also present. MMC firmware was lacking, and a new implementation had to be done by LNLS to better user the board [17]. This is something any in-house project must tackle, but a COTS board user wouldn't expect to deal with it. On the other hand, sharing the design with other laboratories meant we had early support on this development.

ISBN 978-3-95450-189-2

The original board documentation - both design files and manual - were severely lacking in quality. The automatically generated BOM from the design file had to be hand-edited for new production. Variations had to he added to the schematic so we could generate the boards according to our necessities. A complete manual for the AFC hardware and software is yet do be done.

A final note must be done that he board layout is extremely complicated for a board this size: the demand to support several different users and interests means the board has more features than any single user may need. While it does not make the board more expensive, this burdens updates and redesigns of the board.

FMC Digitizer

The merge of the best features of FMC130 and FMC250 is a good example of what can be done with open hardware. While reverse engineering and independent development is always possible, by reusing the actual design, the LNLS team could quickly gather the best features of each board.

One issue in the FMC250 board was the trace and clearance widths of the PCB: the designed employed a minimum of 3mil, and only one Brazilian PCB manufacturer could send us a quote meeting a specification with less than a 4mil width/clearance. A detailed analysis have shown to us this limitation could have been avoided, even though it would require vast layout redesign.

This is a common pitfall between open hardware and other shared projects: a set of constraints decided by a designer in a different context may artificially limit the pool of suppliers an open-hardware user is able to use, or impose extra costs on manufacturing or redesign.

RF Front End

This board was completely designed in-house, and its different versions could not take advantage of any open-hardware project. On the other hand, it ended up being the simplest to build and maintain - by restricting its demands to those of Sirius, it could focus in the sole application.

However, inputs from different engineers in a more open collaboration could have resulted in improvements in the board. The Sirius' partner companies have added several minor improvements to the board, specially in its mechanical parts and electronics form factor. Open hardware built in close collaboration with engineers from other laboratories and companies could have benefited the design from the beginning.

CONCLUSION

Open hardware has enabled fast and highly sophisticated developments by the LNLS team, allowing us to bring a complete BPM electronics system to fruition with limited resources. Contact with existing projects also enable fast learning by the team, enabling newer projects and advances in other areas.

The results of this development has also served as base to other systems at Sirius, such as the orbit feedback and timing system, simplifying the support work for future hardware, firmware and software.

Common issues in open projects have also arose, such as difficult in finding local support and documentation failures that demanded extra work from LNLS. These issues are currently being tackled by the diagnostics team with support of partner companies.

ACKNOWLEDGMENT

The authors would like to thank everyone who helped in the OHWR mailing by discussing the projects, as well as all of those who contributed to the open hardware projects mentioned in this paper. In particular, we would like to thank Rafael Baron, currently at ESS, and Fernando Henrique Cardoso from LNLS for their fundamental contribution to the aforementioned projects.

REFERENCES

[1] A. R. D. Rodrigues *et al.*, "Sirius Status Report", in *Proc. IPAC'16*, Busan, Korea, May 2016, paper WEPOW001, pp. 2811–2813.

[2] CERN Open Hardware License v1.2, Sep. 2013, `http://www.ohwr.org/licenses/cern-ohl/v1.2`

[3] Open Hardware Repository, `http://www.ohwr.org`

[4] J. R. Ackermann, "Toward open source hardware", *U. of Dayton Law Review*, vol. 34, pp.183–222, 2009.

[5] Open Source Hardware Association, "Open Source Hardware (OSHW) Definition 1.0", `http://www.oshwa.org/definition/`.

[6] L. Fried, "Open Source Hardware Licenses", May 2011, `http://www.ladyada.net/library/openhardware/license.html`

[7] AMC FMC Carrier, `http://www.ohwr.org/projects/afc`

[8] Stand-alone 18-slot FMC carrier, `http://www.ohwr.org/projects/sac-18-fmc`

[9] Discussion on OHWR mailing list, Jul. 2012, `http://lists.ohwr.org/sympa/arc/bpm/2012-07/msg00025.html`

[10] Simple VME FMC Carrier (SVEC), `http://www.ohwr.org/projects/svec`

[11] Simple PCIe FMC carrier (SPEC), `http://www.ohwr.org/projects/spec`

[12] µTCA RTM 8 SFP+, `http://www.ohwr.org/projects/utca-rtm-8-sfp`

[13] FMC ADC 130M 16b 4cha, `http://www.ohwr.org/projects/fmc-adc-130m-16b-4cha`

[14] FMC ADC 250M 16b 4cha, `http://www.ohwr.org/projects/fmc-adc-250m-16b-4cha`

[15] S. R. Marques *et al.*, "Status of the Sirius RF BPM electronics", in *Proc. IBIC'14*, Monterey, USA, Sep. 2014, paper WECYB3, pp. 505–509.

ISBN 978-3-95450-189-2

[16] D. O. Tavares *et al.*, "Development of an Open-Source Hardware Platform for Sirius BPM and Orbit Feedback", in *Proc. ICALEPCS'13*, San Francisco, USA, Oct. 2013, paper WECOCB07, pp. 1037–1039.

[17] H. A. Silva and G.B.M. Bruno, "openMMC: An Open-Source Modular Firmware for Board Management", presented at PCaPAC'16, Campinas, Oct. 2016, paper THPOPRPO04, this conference.

ISBN 978-3-95450-189-2