OPERATION EXPERIENCE AND MIGRATION OF I/O CONTROLLERS FOR J-PARC MAIN RING

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Abstract

In 2008, when we started beam commissioning of J-PARC MR, I/O controllers (EPICS IOC) were consisted of about 80 pieces of VME-bus computers and a few PC-based controllers. The total number of IOCs was 80-90.

In 2016, we have non-VME IOCs: a) Yokogawa F3RP61 (Linux-based CPU with PLC I/O modules), b) virtual ioc (EPICS IOC on a virtual machine), and c) commercial micro-server. The total number of IOCs is around 170.

Histories and characteristics of VME and non-VME IOCs are described in this report. In addition, based on operation experience since 2008, reliability of VME-bus computers is discussed.

INTRODUCTION

J-PARC (Japan Proton Accelerator Research Complex) is a high-intensity proton accelerator complex, located in Ibaraki, Japan. It consists of three accelerators: a) 400-MeV Linac (LI), b) 3-GeV Rapid Cycling Synchrotron (RCS), and 30-GeV Main Ring (MR) [1-3]. The control system of J-PARC was developed using the EPICS (Experimental Physics and Industrial Control System) toolkit [4-5].

J-PARC MR started beam operation in 2008. Since then, the beam power of MR has been improved year by year. In June, 2016, the power reached 425kW (Figure 1). We continue beam commissioning toward the design goal, 750kW, and more [6].

To support commissioning activities, the MR control system has been often required to add new beam-diagnostic devices, or follow upgrade of existing power supplies, and so on, in a limited period. Thus, flexibility and extension ability are very important.

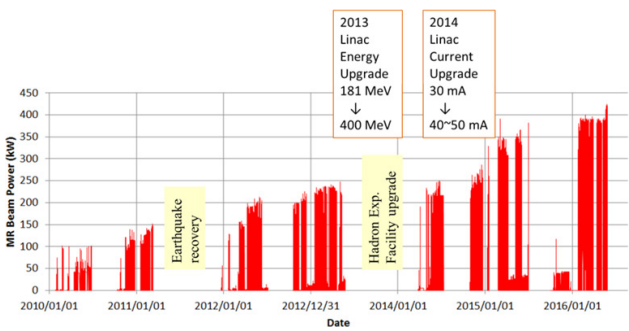

Figure 1: Improvement of MR beam power until 2016.

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CHROCICLE OF IOC IN J-PARC MR

Initial Design of IOC for J-PARC MR

The control system for J-PARC MR was constructed in 2006-2008. At the time, a VME-bus was understood to be robust and highly reliable, compared with other platforms. Thus, we selected VME-bus computer as a primary I/O controller (hereafter IOC). About 80 pieces of VME-bus IOCs were introduced in 2008.

However, in our history, non-VME-type IOCs were also introduced. Even in 2008, a PC-based controller was introduced. Then, a PLC-type Linux-based CPU in 2009, an IOC running on a virtual machine in 2011, and a commercial micro-server ("Saba" IOC) in 2015, were introduced. The numbers of MR IOCs between 2008 and 2016 are summarized in Figure 2.

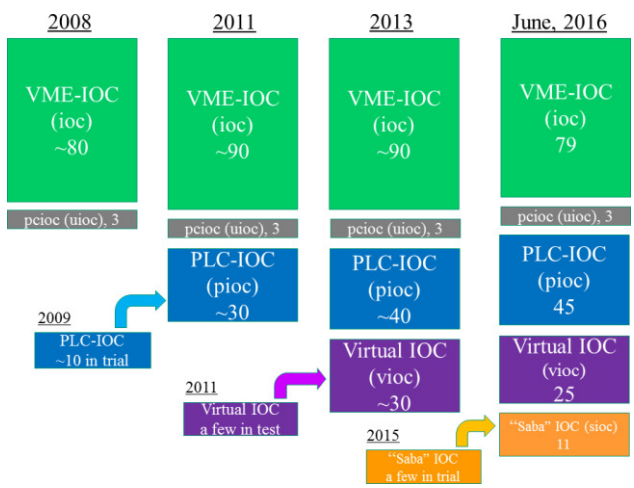

Figure 2: Numbers of MR IOCs between 2008 and 2016.

VME-IOC and PC-based IOC

In 2008, three (later four) models of VME-bus computers were used in MR operation: (a) the model, VMIC V7807 (after 2009, V7865), for DAQ of network-based digitizers (Yokogawa WE7000) [7], (b) the model, Sanritz SVA041, for controlling ladder-logic PLC (Yokogawa FA-M3) [8], and (c) the model, VMIC V7700, for VME-bus timing modules [9]. The specs of four models are given in Table 1. For all the models, we selected Intel-based chip, in order to run Linux OS. Front-end devices underneath VME-IOCs are shown in Figure 3.

One model of vacuum controllers has no external control interface but a RS485 port. It was not supported

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by VME-IOC. Thus, we decided to introduce a "microIOC", a customized PC-based controller provided by Cosylab [10]. A model with eight RS485 ports was introduced (Figure 4).

Table 1: VME-bus CPU modules in J-PARC MR

CPU Model	Device	Spec
VMIC V7807	Digitizer (TCP/IP)	Pentium M, 1.8GHz 1.0/1.5GB memory
VMIC V7865	Same as above # After 2009	Core Duo T2500 2C2T 2.0GHz / 3GB
Sanritz SVA041	Ladder PLC (TCP/IP)	ULV Celeron M 600MHz / 512MB
VMIC V7700	timing modules (VME-bus)	Celeron M 400MHz / 512MB

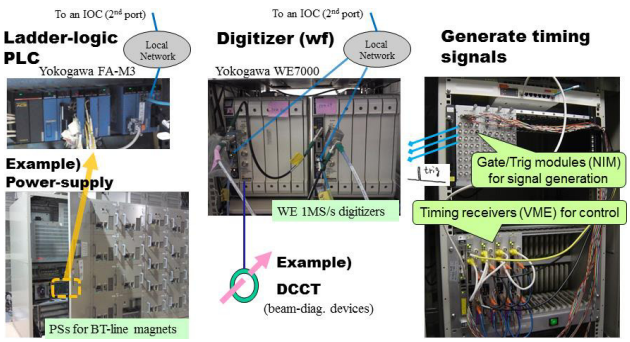

Figure 3: Front-end devices underneath VME-IOCs.

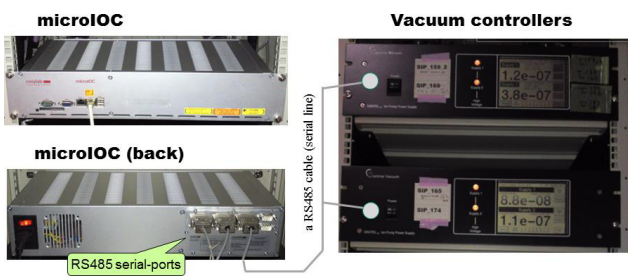

Figure 4: A microIOC and vacuum controllers.

PLC-IOC

In 2008, porting EPICS into F3RP61 (a Yokogawa's Linux-based CPU for PLC) was carried out by KEK and RIKEN [11-12]. As in Figure 5, this enabled us a "PLC-IOC", which uses robust PLC I/O modules without ladder programming and a separated VME-IOC. After 2009, many PLC-IOCs, each consists of a F3RP61 and suitable I/O modules, have been introduced in J-PARC MR [13-14]. A PLC-IOC for octapole magnets is a typical example (Figure 6).

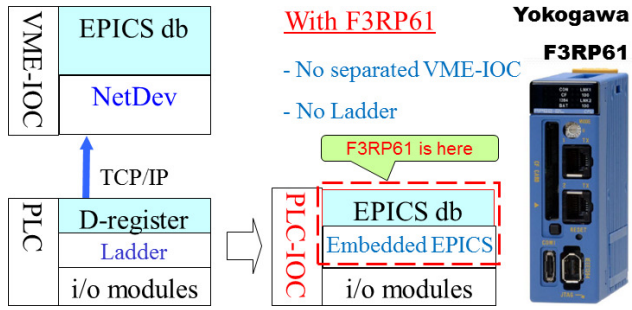

Figure 5: Scheme of PLC-IOC with a F3RP61.

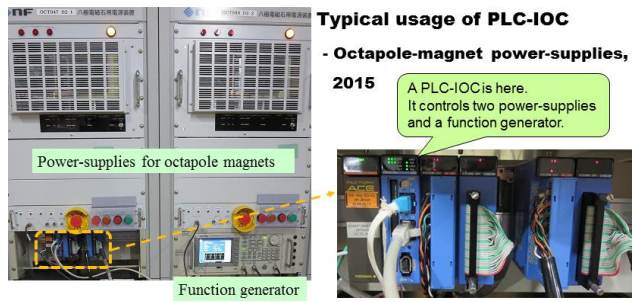

Figure 6: A PLC-IOC to control octapole magnets.

Virtual IOC

The "virtual IOC" is an EPICS IOC running on a virtual machine. Since 2011, virtual IOCs have been used for network-based devices, and soft-IOCs of management purposes. Three blade-type servers, with Scientific Linux 6.7 and KVM, have been used as host machines [15-16].

Example of virtual IOCs in MR are shown in Figure 7. The left is a network traffic monitor using the SNMP protocol. The right provides an automatic tuning of digitizer scales at parameters changes. In the right case, a virtual IOC communicates with three "real" IOCs.

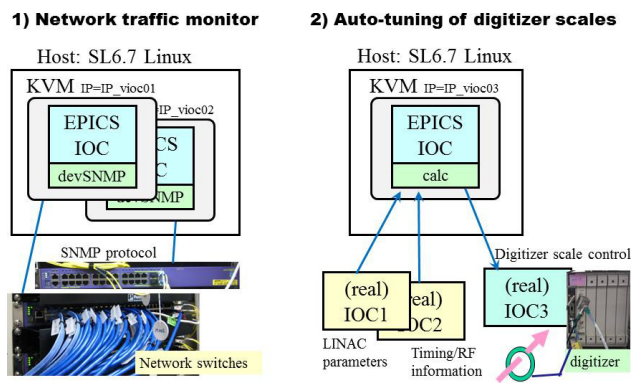

Figure 7: Two examples of virtual IOCs in J-PARC MR.

"Saba" IOC

The "Saba Taro" is a commercial micro-server. It is designed for administrative purposes (i.e. DNS, Web, DHCP, etc.) used in a small office, or for a host of IoT devices [17]. A "Saba" IOC is an EPICS-IOC, using a

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"Saba Taro" of the model "Pinon Type-P" [18]. A "Saba" IOC is much cheaper and much smaller, however, much powerful than a VME-IOC. Figure 8 shows the spec of "Saba Taro" and some of VME-IOCs in comparison.

A VME-IOC for network-based devices can be replaced by a "Saba" IOC. In 2015, we carried out a reliability test of a few "Saba" IOCs in MR field areas. They ran without any trouble over a year. In 2016, we start a multi-year plan to replace VME-IOCs by "Saba" IOCs, gradually in the coming years (Figure 9).

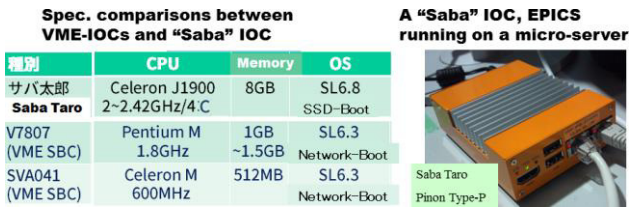


Figure 8: A "Saba" IOC and its spec.

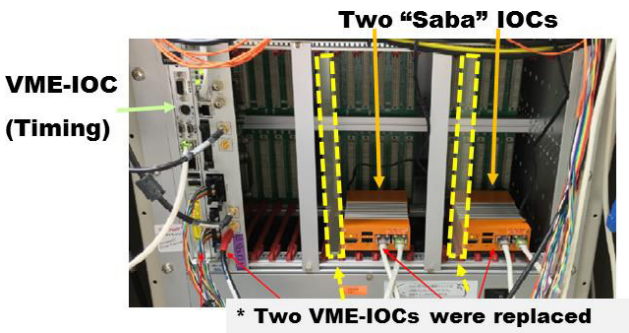


Figure 9: Two VME-IOCs were replaced by "Saba" IOCs.

DISCUSSION

Number of J-PARC MR IOCs in 2016

In June, 2016, numbers of various IOCs used in J-PARC MR operation are summarized in Table 2.

Table 2: List of IOCs in June, 2016 in J-PARC MR

IOC type	Number	Interface (Purpose)
VME-IOC (V7807, V7865,SVA041)	54	Network (digitizer, ladder-PLC)
VME-IOC (V7700)	25	VME-bus (Timing)
PC-based IOC	3	RS485 (Vacuum)
PLC-IOC	45	Basic signal I/O
Virtual IOC	25	Misc.
"Saba" IOC	11	Network

Reliability of VME-bus Computer

During 2008-2011, VME-IOCs worked well without troubles. Since 2011, each time after a scheduled power outage, a few VME-IOCs did not run. On-board memory card was broken (Figure 10). After replacing the broken card by a spare, the VME-IOC worked again. Memory cards on the models SVA041 and V7807 were broken, however, no failure on other models. Number of broken cards at each power outage is shown in Figure 10.

Later, we knew that all broken memory cards are the products in the middle of 2007. We introduced 33 (22) pieces of SVA041 (V7807) in 2007. Until 2016, 20 of 33 memory cards on SVA041 (7 of 22 on V7807) were broken, respectively. More detailed analysis on this issue is given elsewhere [19].

In 2015, Micron, a DRAM company, announced a defect in DRAM chips which were shipped before December, 2010 [20]. Figure 11 is an essential part of the announcement. Observed our problem is well understood.

It is worth noting that no trouble on main VME boards of the models, SVA041 and V7700, since 2008. In addition, VME boards introduced not in the middle of 2007 have no memory card failure. However, this experience arise a suspicion for reliability of VME-bus computers, and encourages us to use "Saba" IOCs more.

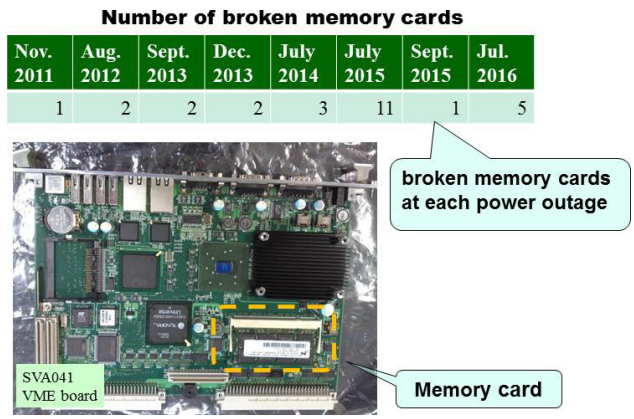
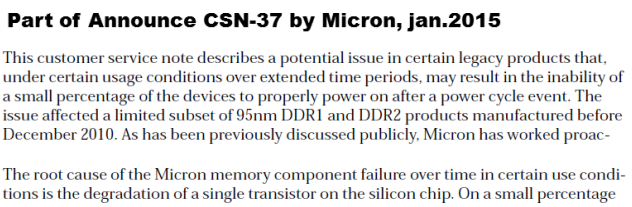


Figure 10: Memory card failures during 2011 and 2016.


Part of Announce CSN-37 by Micron, jan.2015

This customer service note describes a potential issue in certain legacy products that, under certain usage conditions over extended time periods, may result in the inability of a small percentage of the devices to properly power on after a power cycle event. The issue affected a limited subset of 95nm DDR1 and DDR2 products manufactured before December 2010. As has been previously discussed publicly, Micron has worked proac-

The root cause of the Micron memory component failure over time in certain use conditions is the degradation of a single transistor on the silicon chip. On a small percentage

Figure 11: Part of the announcement by Micron.

CONCLUSION

Various types of I/O controllers of J-PARC MR are reviewed. Based on the operation experiences between 2008 and 2016, reliability of VME-bus type I/O controller is discussed.

We appreciate all the MR staff members for their continuous efforts to maintain and update I/O controllers.

REFERENCES

[1] J-PARC website: http://j-parc.jp/index-e.html

ISBN 978-3-95450-189-2

[2] S. Nagamiya, "Introduction to J-PARC", *Prog. Theor. Exp. Phys.* 2012 02B001.

[3] T. Koseki and K. Hasegawa, "Present Status of JPARC - After the Shutdown due to the Radioactive Material Leak Accident -", in *Proc. IPAC'14*, Dresden, Germany, paper THPME061, pp.3374-3375.

[4] `http://www.aps.anl.gov/epics/`

[5] N. Kamikubota *et al.*, "J-PARC Control toward Future Reliable Operation", in *Proc. ICALEPCS'11*, Grenoble, France, Oct. 2011, paper MOPMS026, pp. 378-381.

[6] S. Igarashi, "Recent Progress of J-PARC MR Beam Commissioning and Operation", in *Proc. HB2016*, Malmo, Sweden, July 2016, paper MOAM6P60, pp. 21-26.

[7] M. Takagi *et al.*, "Linux Support of WE7000 EPICS Driver for J-PARC MR", in *Proc. of 3rd Annual Meeting of Particle Accelerator Society of Japan*, Sendai, Japan, Aug. 2006, pp.448-450.

[8] J. Odagiri *et al.*, "Development of EPICS Device/Driver Support Modules for Network-based Devices", in *Proc. of 3rd Annual Meeting of Particle Accelerator Society of Japan*, Sendai, Aug. 2006, pp.925-927.

[9] N. Kamikubota *et al.*, "Operation Status of J-PARC Timing System and Future Plan", in *Proc. ICALEPCS'15*, Melbourne, Australia, Oct. 2015, paper WEPGF121, pp.988-991.

[10] `http://www.cosylab.com/microioc/`.

[11] A. Uchiyama *et al.*, "Development of Embedded EPICS on F3RP61-2L", in *Proc. PCaPAC'08*, Ljubliana, Slovenia, Oct. 2009, paper WEX03, pp. 145-147.

[12] J. Odagiri *et al.*, "Application of EPICS on F3RP61 to Accelerator Control", in *Proc. ICALEPCS'09*, Kobe, Japan, Oct. 2009, paper THD005, pp. 916-918.

[13] M. Takagi *et al.*, "Control of the J-PARC Slow Extraction Line based on Embedded EPICS", in *Proc. ICALEPCS'09*, Kobe, Japan, Oct. 2009, paper WEP076, pp.549-551.

[14] S. Motohashi *et al.*, "Data Acquisition System of Beam Loss Monitors of the J-PARC Main Ring", in *Proc. ICALEPCS'09*, Kobe, Japan, Oct. 2009, paper WEP070, pp. 537-539.

[15] N. Kamikubota *et al.*, "Virtual IO Controller at JPARC MR using XEN", in *Proc. ICALEPCS'11*, Grenoble, France, Oct. 2011, paper WEPMU039, pp. 1165-1167.

[16] N. Kamikubota *et al.*, "Experience of Virtual Machines in J-PARC MR Control", in *Proc. ICALEPCS'13*, San Francisco, CA, USA, Oct. 2013, paper MOPPC131, pp. 417-419.

[17] `http://www.pinon-pc.co.jp/hp/?page_id=102`

[18] S. Yamada, "Deployment of a tiny fanless server as IOC in J-PARC Main Ring", in *Proc. of 13th Annual Meeting of Particle Accelerator Society of Japan*, Chiba, Japan, Aug. 2016, MOP092, in press.

[19] N. Kamikubota *et al.*, "J-PARC MR's Experience on VME-bus Computers in the Last Decade", in *Proc. of 13th Annual Meeting of Particle Accelerator Society of Japan*, Chiba, Aug. 2016, MOP095, in press.

[20] `https://www.micron.com/~/media/documents/products/customer-service-note/csn37_95nm_legacy_dram.pdf`

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