THE TNK BEAM POSITION MONITOR SYSTEM

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Abstract

New second generation synchrotron radiation source TNK is being built in Zelenograd, Russia. The new FPGA-based beam position monitor (BPM) system for TNK has been developed and produced in BINP. The BPM system requirements for second generation light sources are not as severe as for the third generation light sources. Nevertheless the system is able to perform turn-by-turn measurements and has micron level accuracy. The TNK light source is intended for work both in multiple and in single bunch mode. In the second case the charge of one bunch can achieve the value of 60 nK, which results in high peak voltages at BPM electrodes. Design features of the BPM system, its parameters and testing results are presented in this paper.

INTRODUCTION

Second generation synchrotron radiation source TNK ("Zelenograd") is presently under construction in Zelenograd, Russia [1]. Storage ring main parameters are given in Table 1.

Table 1: Main parameters of the TNK storage ring

Beam energy	2 GeV
Revolution frequency F_0	2.59 MHz
RF frequency	181.3 MHz
Beam current in multiple bunch mode	300 mA
Beam current in single bunch mode	150 mA

For beam orbit measurements Beam position monitor (BPM) system has been designed and fabricated at BINP. The system includes 24 button-type Beam Position Monitors (BPMs) and BPM electronics. Requirements to BPM electronics are:

- possibility of turn-by-turn measurements
- measurements of injected beam trajectory (first turn)
- resolution for nominal beam currents not worse than 1-2 microns
- relative accuracy for nominal beam currents at ~10 microns
- measurement rate is ~10 Hz, fast data acquisition is not required.

Slow data acquisition (~10 Hz) will be used for slow orbit feedback. Fast orbit feedback is not planned at TNK.

SYSTEM STRUCTURE

One of the methods which combine turn-by-turn measurements with high accuracy is method based at the use of an array of switches [2]. We choose this method for our BPM electronics. One of the problems associated with the use of semiconductor switches was high peak voltages at pickup buttons. In single bunch mode the charge of one bunch can achieve the value of 60 nK which gives peak voltage of tens of volts after passing through Low Pass Filter with cut-off frequency of 500-600 MHz.

Acceptable solution of this problem is employment of RF band pass Filters (BPF) directly after pickup buttons [3]. For this purpose a special printed-circuit BPF with frequency 362 MHz (doubled RF frequency) had been developed at BINP. The measured parameter S_{21} of the filter is shown in Fig.1,2. The measured bandwidth is ~10 MHz, insertion loss is ~6 dB.

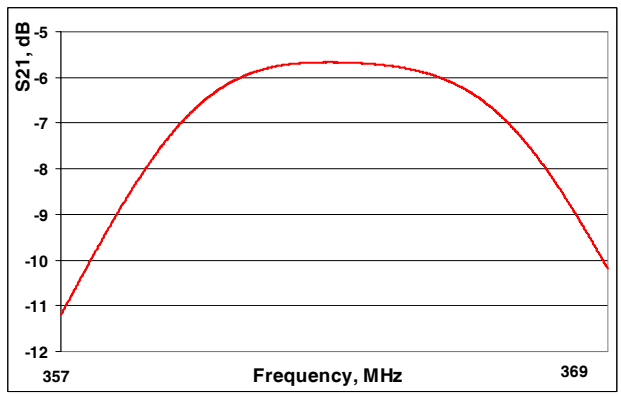

Fig.1. Measured S_{21} of BPF, narrow frequency span.

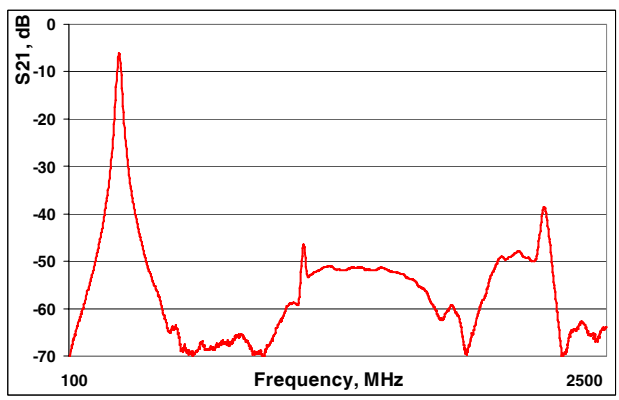

Fig.2. Measured S_{21} of BPF, wide frequency span.

Inequality of Band Pass Filters results in static measurement error therefore calibration of electronics is needed.

The structure of the BPM electronics is presented in Fig.3.

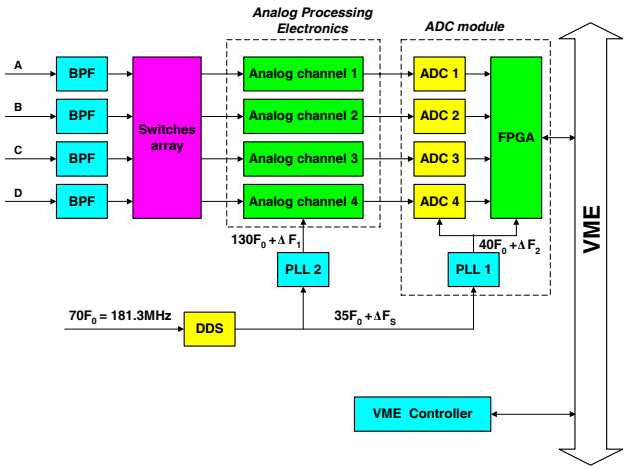

Fig.3. The structure of the BPM electronics.

Second harmonic of RF frequency $140F_0$ (362.6 MHz) is extracted from BPM signal and used for measurements.

GaAs switches provide 4 combinations of connections between 4 pickup buttons and 4 analog channels. Channel to channel crosstalk is less than -60 dB.

Analog Processing electronics occupy 1U 19" chassis. After analog processing the signals via 50 Ohm cables come to ADC module (made in VME standard) where are sampled. One ADC module contains four 14-bits ADCs, FPGA and clock generator (PLL).

Digital signal processing is performed in FPGA. The results are transmitted via VME bus to VME Controller.

ANALOG AND DIGITAL SIGNAL PROCESSING

A functional diagram of the analog signal processing channel is presented in Fig.4.

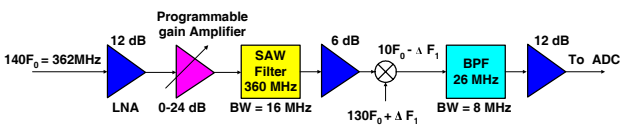

Fig.4. Functional diagram of the analog processing channel.

The signals with a frequency of $140F_0$ after amplification by Low Noise Amplifier (LNA) and Programmable Gain Amplifier are mixed with heterodyne signal. Band Pass Filter (SAW filter) with bandwidth of 16 MHz minimizes noise and distortions and provides additional suppression of mirror components. The heterodyne frequency differs from $130F_0$ by a small value of ΔF_1 (a few kHz), so after mixing the signal frequency becomes $10F_0 - \Delta F_1$. Offset of the heterodyne frequency from integer multiple of revolution frequency provides insensitivity of result from signal phase. The signals selected by Band Pass Filter with central frequency of 26 MHz and bandwidth of 8 MHz are then amplified and pass to ADC module where they are sampled at frequency of $40F_0 + \Delta F_2$.

ADC sampling frequency also slightly differs from integer multiple of revolution frequency. This compensates some of the undesirable effects caused by nonlinearity of ADC and other components [3]. Offsets ΔF_1 and ΔF_2 improve resolution of measurements, decrease fill-pattern dependence and make the result insensitive to signal phase. It is especially important for single bunch mode.

Heterodyne and sampling frequencies are generated by low jitter Phase Locked Loop (PLL) oscillators AD9516. Specified time jitter of this oscillator in a bandwidth of 0.01-20 MHz is 0.275 ps. Reference frequency for both PLLs is generated by Direct Digital Synthesizer (DDS) AD9958. DDS frequency ($35F_0 + \Delta F_S$) defines ΔF_1 and ΔF_2 values. Reference frequency for DDS is RF frequency 181.3 MHz. Because of comparatively large DDS phase noise PLL loop bandwidth is chosen 1 kHz. As a consequence DDS phase noise at frequencies more than 1 kHz is not transferred to oscillators. Measured heterodyne jitter in bandwidth 0.1-100 MHz is less than 1 ps.

Digital signal processing chain in FPGA is shown in Fig.5.

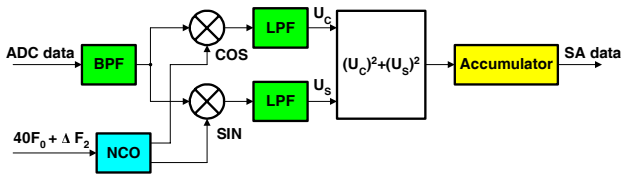

Fig.5. Digital signal processing chain.

Numerically Controlled Oscillator (NCO) frequency slightly differs from $10F_0$. It is calculated on base of ΔF_1 and ΔF_2 values so that data after synchronous detector is a DC value. A sum of squares of Sin and Cos components is calculated for each turn. Then these values are accumulated for specified number of turns to form Slow data acquisition (SA). As a consequence low frequency phase noise (less than 100 kHz) does not worsen resolution of measurements.

EXPERIMENTAL TESTS RESULTS

BPM electronics had been tested at test stand and at BINP storage ring VEPP-4M.

At test stand Agilent Signal Generator and Agilent Pulse Generator where used as signal sources modeling multi bunch and single bunch modes. The signals of these generators where split into four lines. A -3dB attenuator was inserted into one of the lines to imitate beam displacement. Five main parameters where measured at test stand:

- Resolution
- Temperature instability of the beam position measurements
- Beam-current dependence
- Fill-pattern dependence

- Dependence on the signal phase for single bunch mode

All BPM electronics hade been investigated. Results are given in Table 2. Geometric factors of BPMs: K_X=K_Z=20 mm.

Table 2: BPM system parameters defining accuracy of measurements (K_X = K_Z = 20 mm) for average beam current 50÷300mA (pickup signal level: -14÷2 dBm).

Resolution of slow measurements (SA data)	µm	0.2-0.5
Resolution of turn-by-turn data	µm	8-10
Beam-current dependence	µm	< 10
Fill-pattern dependence	µm	< 15
Dependence on bunch phase for single bunch mode	µm	< 5
Temperature dependence	µm/°C	1.5-2

Relatively large dependence of the result on temperature (1.5-2 µm/°C) is caused by two reasons:

- Inequality of the Band Pass Filters (input BPF)
- Inequality of Ga As switches.

Different temperature dependencies of insertion loss of different BPFs and switches results in temperature dependence of the measurement result. Nevertheless these results satisfy of machine requirements. Special thermal stabilization is not needed.

Results of measurements during 2 hours at test stand for one of sets of electronics are given in Fig.6. Resolution of ~0.2 µm was achieved. Slow changing of result is caused by temperature instability.

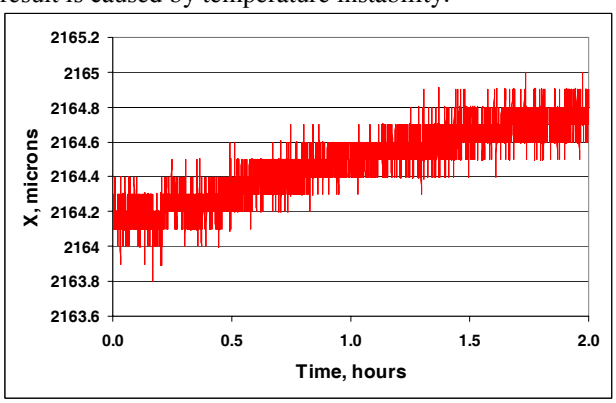

Fig.6. Results of measurements at test stand with signal level of -10 dBm.

Results of measurements during 1 hour at VEPP-4M storage ring with small beam current ~2 mA and data rate 1 Hz are presented in Fig.7 (K_X = K_Z = 43 mm).

Root-mean-squire deviations of measured horizontal and vertical positions are ~3 µm and ~1 µm correspondingly. Some part of these values is caused by real beam position instability.

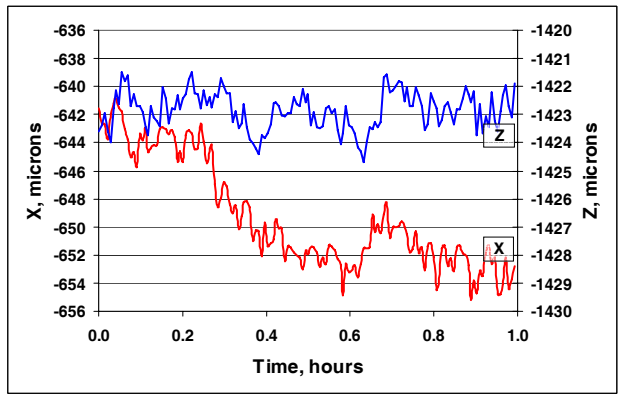

Fig.7. Results of beam position measurements at VEPP-4M with beam current ~2 mA (signal level of -45 dBm).

STATUS

At present all 24 BPMs have been manufactured and installed at TNK storage ring. All electronics has also been made, tested and calibrated at test stand. 80 % of electronics satisfy machine requirements. Remaining part needs additional tuning. Commissioning of BPM system at TNK is planned at first half of 2011.

REFERENCES

[1] Salashenko at al. “Status of “Zelenograd” storage ring”. Nuclear Instruments and methods in Physics research. Volume 603, p.4-6.

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