

UNIVERSAL TIMER MODULE FOR THE TIMING SYSTEM OF THE ACCELERATING STORAGE COMPLEX ITEP-TWAC

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Abstract

A multipurpose synchronization module for renovating timing system of ITEP-TWAC accelerator facility is developed. A group of such modules is aimed to implement a sophisticated set of synchronization functions among four accelerators – proton LINAC I2, ion injector I3, buster synchrotron UK and accelerating and storage ring U10. This FPGA based module generates up to 16 output pulses related to timing scale (T), magnetic field scale (B), radio frequency, external events or their combination. The read back function allows controlling the pulses propagation on cycle-to-cycle basis. The structure of the module, a description of basic functions and IO interface are presented in details. Also an example of system configuration based on the developed module is discussed.

INTRODUCTION

The modernization of an accelerating complex in ITEP [1] lays new demands to the synchronization of the systems of accelerators. A new timing system should work with increasing number of synchronous elements providing more and more functionality and flexibility.

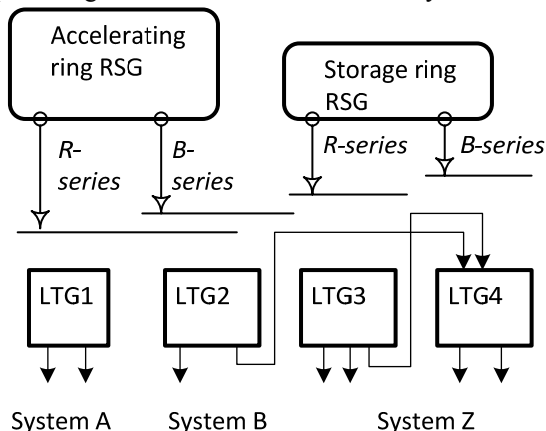


Fig. 1. A principle of organization of the timing system of the ITEP’s accelerators

A principle of synchronization of the ITEP’s accelerating complex shown on fig. 1.

Reference devices (reference signal generators RSG) generate **B**- and **R**- sequences of pulses synchronous to the magnetic field strength and zero phase of RF oscillations. Followed local timing generators LTGs are an assembly of properly commuted logical modules, modules of programmable time delays and fan-out modules as it shown on fig. 2. The system has a multiple hierarchy levels and distributed over the area. Some local generators are realized in the form of standalone units,

synchronized by one or two pulses from higher-level LTG. Some of local generators are placed outside of the synchrotron’s control room. There are, for instance, timing systems of proton or ion sources. This allows an independent work of linacs on their own targets.

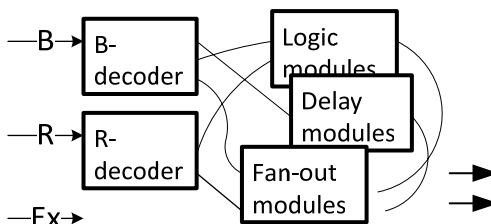


Fig. 2. A Local Timing Generator synchronizes devices with magnetic field (B), RF phase (R) and/or external events (Ex).

The tasks of the developing timing system are, in particular, unification of used modules, simplification of the process of the system setting up and extending of a system’s functionality. The concept of the new timing system is based on the experience of the exploitation of the existing system in ITEP as well as other similar systems in GSI and CERN. A new timing system concept for CERN and FAIR so-called White Rabbit project [2] also has been examined. Similar to the White Rabbit the future timing system of ITEP presumed a possibility of precise delay compensation over Ethernet. But in opposition to White Rabbit, ITEP keeps a dedicated serial timing bus STB (fig.3b). The synchronized Ethernet (IEEE 1588) is an option, which is used when it is necessary without any modification of general standard. This way looks more reliable and budgetary which has the sense in present-day situation. Nevertheless, we are looking forward and in the case of successful realization of the White Rabbit project and the appearance of commercial accessible components there is a possibility of the essential incorporation of this new technology into the developed system.

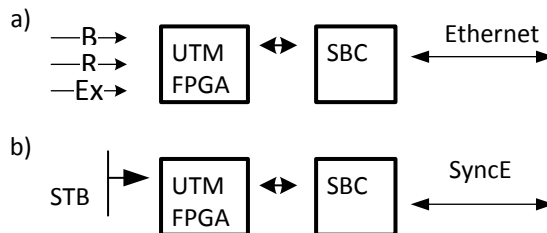


Fig. 3. Applications of the UTM: replacement of existing modules on top, using serial timing bus STB and synchronization over Ethernet on bottom.

A universal timing module UTM was developed as a key component of a new system. It intends to smoothly

replace existing timing elements in the way, shown on fig. 3.a. In the same time the UTM is a part of new technology required to fulfill new demands. It is ready to be used jointly with contemporary elements and structures like synchronized Ethernet (fig. 3b).

STRUCTURE AND THE FUNCTIONAL POSSIBILITIES OF THE UNIVERSAL MODULE

The logical structure of the module is shown in fig. 4. Element density of the contemporary programmed logic makes it possible to place several local timing generators in the single universal module. Functional modules FG give a possibility to generate complex sequences of pulses at the outputs of the device. A serial timing bus decoder's standard component is including into firmware when it is necessary to operate with STB. As a standard option, it is also possible to compensate a cable delay. A correction component, shown on the figure, could be set up after manual calibration or during automatic calibration by synchronized Ethernet.

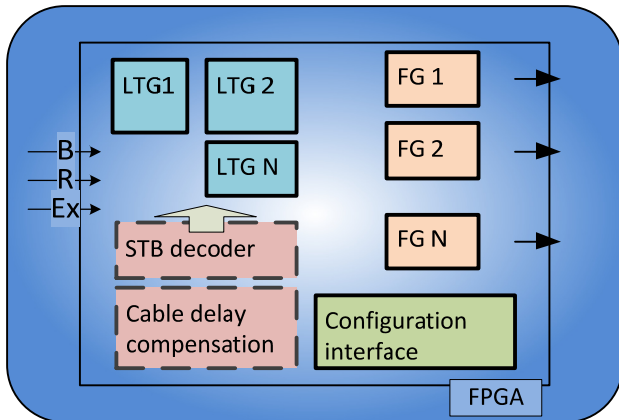


Fig. 4. Logic of the universal timer module realizes several LTG, a collection of functional blocks and series of specialized components. Numerous interfaces allow connecting via serial or parallel bus (RS485, PC104).

The accelerating facility of ITEP has different operating modes, therefore the timing must support all of them. Basic event markers for the timing system are given in fig. 5.

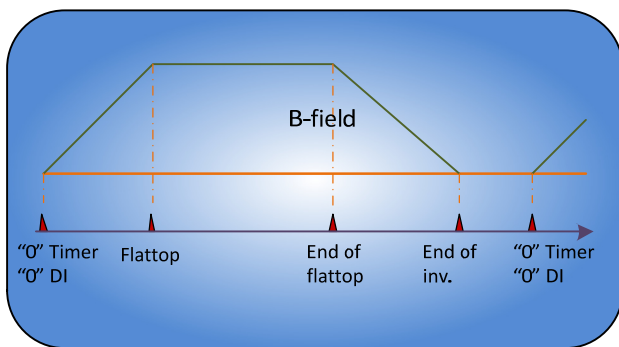


Fig. 5. Cycle of acceleration and basic event markers

Fig. 6 presents one of possible modes of operation of the timing system. The ion beam injected to and extracted from accelerating ring while rising magnetic field. A timing module starts the cycle by initiating of LEBT optics elements and main thyristor rectifier. Injection and extraction proceed when the magnetic field reaches predefined values. To initialize the extraction the module predicts magnetic field and issues HEBT start pulse little ahead of the kicker magnet start. To control timing uncertainties in technological systems the module has programmable time windows according required tolerances.

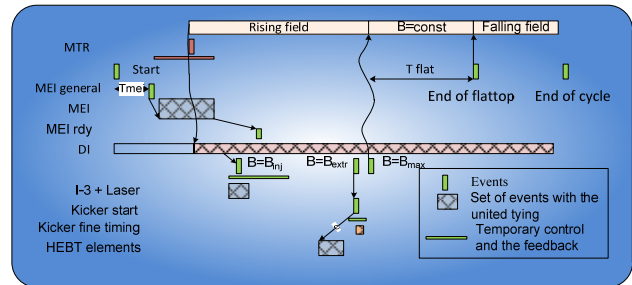


Fig. 6. A typical regime of the work of the timing system of an accelerator. Beam injected into rising magnetic field.

Abbreviations on fig. 6 are: MTR - main thyristor rectifier; MEI - magnetic elements of ion guide; MEI rdy - virtual moment of the maximum current in MEI; DI - discrete integrator, the instantaneous value of magnetic field; Kicker of fine of timing - forming by the external scheme of the precision sequence of trigger pulses with the tying to the phases HF field; HEBT - high energy beam transfer line, ionic optics of transitional channel.

REALIZATION OF THE MODULE

At the present the timing system of the accelerating facility is based on the discrete modules, similar to the one, shown on fig. 7.

The great disadvantage of such blocks is a necessity of a manual commutation while reconfiguration process.

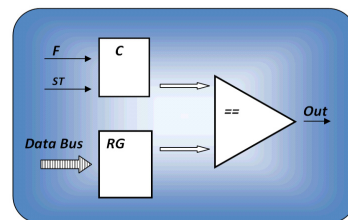


Fig. 7. A discrete block example. F – an internal frequency of 10 kHz or 10 MHz, either external frequency from the discrete integrator of the magnetic field signal or the zero-crossing pulses of the accelerating field. ST- starting of counter. Data bus - external data and address bus. Out - output of the block.

Figure 8 shows components of the UTM. On the bottom there is a single-board computer with Debian

Linux OS. It provides a remote control over Ethernet, a non-volatile storage for system setting and system default set-up during startup process. A dedicated program could be used to provide timing parameters correction in a feedback mode.

Timer module is created on the base of the microchip of the programmed logic FPGA. Use of FPGA makes possible a realization in one module of sixteen 32bit timers with programmable delay values. The selection of the counting and synchronization sources for each of sixteen timers is performed by program by setting a bitmask of an appropriate register. Four counter inputs and a 50MHz on-board oscillator could be used as counting sources. Another four inputs serve for synchronization purpose. Any input and any timers outputs could be used as a synchronization source for any timer internally. All inputs are equipped with protection and normalizing scheme. Also in the module includes a generator with the programmable period and control scheme, which makes it possible to measure the time intervals to control the time of occurrence of various events. Eighteen outputs of module can be independently commuted with the output of any of sixteen timers or with the output of the programmed generator.

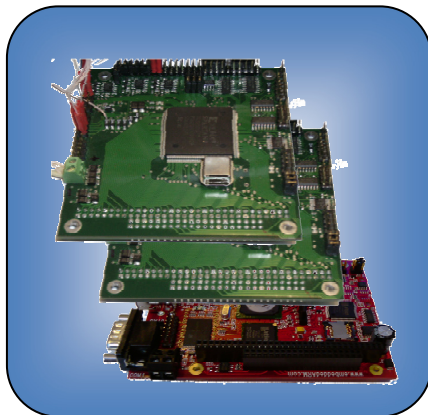


Fig. 8. Timer block, which consists of one single-board computer and two timer modules

Timer module as well as a single-board computer has several RS485 and RS232 ports, furthermore single-board computer has an Ethernet 10/100 and USB 2.0 connectors, the presence of these ports allows additional possibilities to create a distributed timing system with the use of both of the timer blocks and the separate timer modules (fig. 9).

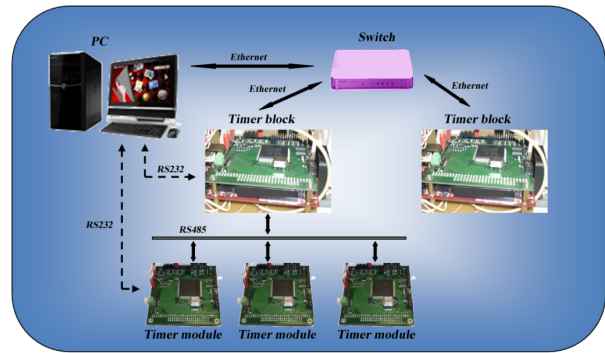


Fig. 9. Example of the creation of the distributed timing system based on timer blocks and discrete timer modules.

CONCLUSION

The Universal Timing module showed a good suitability for solving various timing problems. Behind of operation in ITEP's synchronization scheme it is used in GSI as a timing module for Ionization Profile Monitor [4][5] and as a GSI-to-CERN timing format converter in the frame of FAIR project preparations. The test exploitation of UTMs as a part of the accelerator's timing system showed the complete readiness of the module. Next stages include the reproducing of modules, the development of corresponding software and the smooth adoption of modules into the operating system.

LITERATURE

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