DEVELOPING OF THE SYNCHRONIZATION SYSTEM FOR ACCELERATION-STORAGE FACILITY ITEP-TWAC

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Abstract

The renovation of the ITEP-TWAC synchronization system is a complex and challenging matter. This system must provide a full-scale timing signal set for all existing and foreseeing modes of operation of the two-ring accelerator facility. The workflow of the complete design covers all levels of a design management hierarchy like decision concerning, the new system architecture or basic electronic modules development. In this article we present a description of most critical elements of the synchronization system.

INTRODUCTION

Two general rules were formulated before starting the design of the novel synchronization system. Those rules are following:

- New elements must be compatible with existing system. Partly they are replacing obsolete components giving them where it is necessary a new functionality. A principle of organization of the synchronization system in ITEP-TWAC accelerating complex could be illustrated by Fig.1.

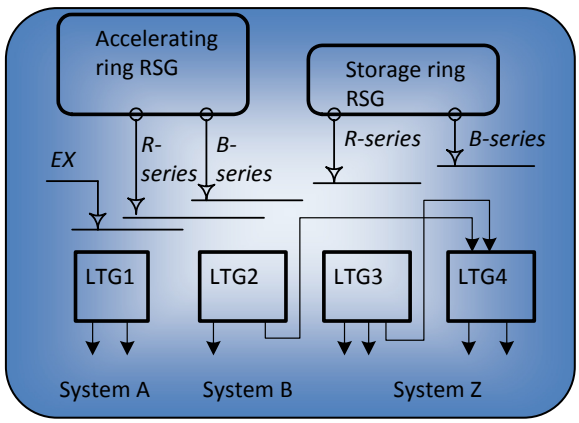

Figure 1.A structure of the synchronization system of the ITEP-TWAC accelerating complex.

- Reference signal generators (RSG) issue so called B- and R- sequences of control pulses which are synchronized with magnetic field strength (B) and RF oscillations(R). The system also accepts external synchronization signals (EX) from independent or adjusted installations like injector and target systems. A general module of the local timing generator LTG is an assembly of logical modules, programmable time-delay modules and signal duplication modules.
- New elements provide possibility to upgrade to the new principles of organization of the synchronization system, namely using serial timing bus (STB) for building synchronization system. A principle of organization of the synchronization system based on STB shown on Fig.2.

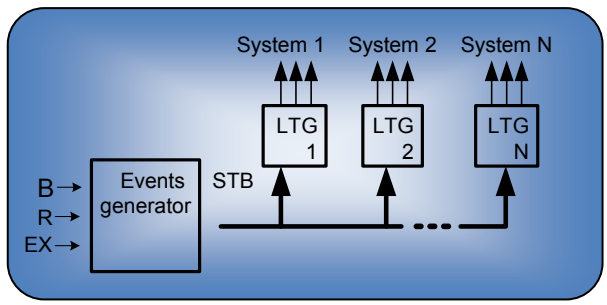

Figure 2. A principle of organization of the synchronization system based on serial timing bus architecture - STB.

STRUCTURE OF THE DEVICES

There are two families of devices, which require for building of the synchronization system with serial timing bus. The first type is a master or event generator shown in Fig.3. The master analyses incoming events of different format on B,R and EX lines and generates unified data frames on the serial bus. The second type is a service module shown on Fig.4.

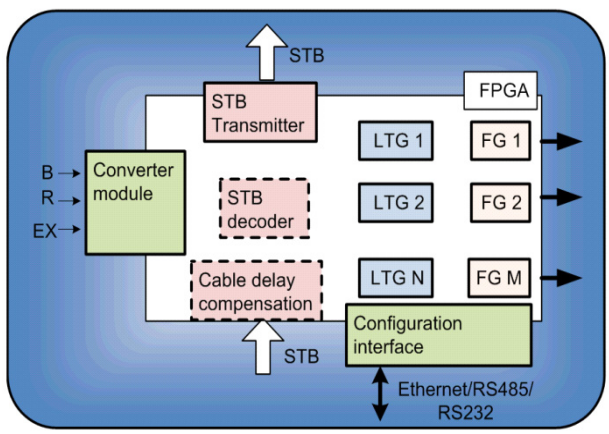

Figure 3. The block scheme of the events generator.

The differences between those two types of devices are nominal because the logical structure of the STB transmitter(master) can be completely realized inside FPGA, except the physical interface of the STB. A service module also can be logically implemented inside FPGA, except the schematic of the input signal converter. Both modules can be realized in the same hardware, therefore

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the module behavior depends only from the micro program loaded into the device.

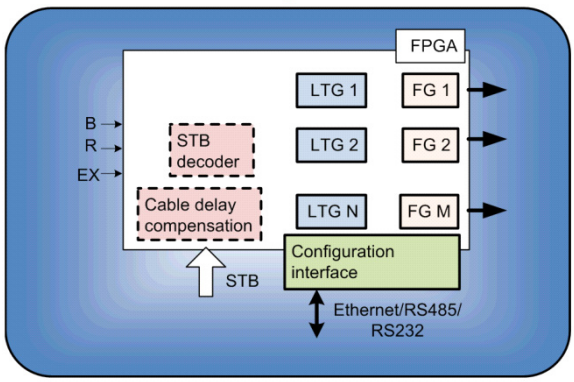

Figure 4. The block scheme of the service module.

The complexity of the contemporary programmed logic makes it possible to place several functional blocks in the single universal module. Functional modules FG give a possibility to generate comprehensive sequences of pulses at the outputs of the device. A serial timing bus decoder's standard component is including into firmware when it is necessary to operate with STB. As a standard option, it is also possible to compensate a cable delay.

DEVELOPMENT OF THE DEVICES

Presently several devices are developed to be used in synchronization system, they are presented below in chronological order. All of the following devices are designed to work with STB which based on RS485 or GSI standard (MIL-STD bus variation) physical interface.

The first of the developed devices is the synchronization module with "Configurable interface" based on single-board Linux computer TS 7800 equipped with extension cards built in PC104 standard. Such module and two extension cards are shown on Fig. 5.

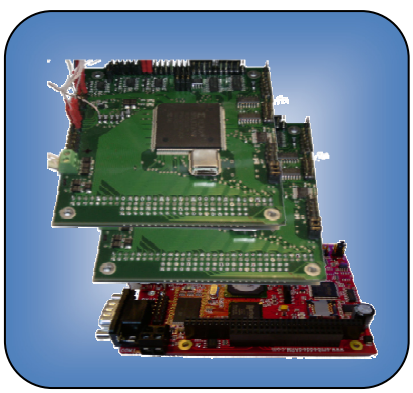

Figure 5. Synchronization module based on single board computer TS 7800.

This solution has several advantages:

- A wide range of physical interfaces RS485, MIL-STD Bus, RS232, USB2.0 and Ethernet 10/100 provide wide opportunities for construction and configuration of the synchronization system. PC104 bus is an easy way to add extension cards, which in their turn provides good scalability and functionality of the module as a whole.
- High computation power of the single-board computer together with possibility of using specialized extension cards for example ADC cards or specific interface cards provides the possibility to use this module as events generator module for synchronization system.

The synchronization system of the linear heavy ion accelerator I4, which is a latest linac built in ITEP, has been designed with use of this module. One module, shown on Fig.5. includes 20 LTG and FG and provides the synchronization of all subsystems of the accelerator.

The next module, which was developed for the synchronization system, is a single board computer based on ARM 7 core processor. This module shown on Fig. 6.

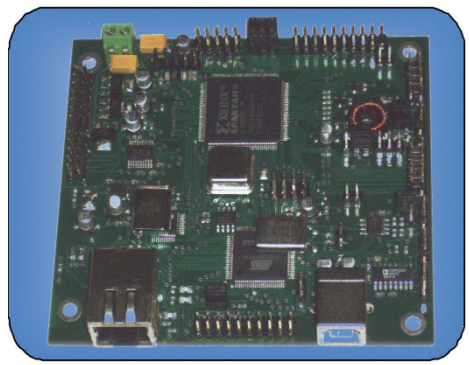

Figure 6. Synchronization module based on single board computer with ARM7 core processor.

In comparison with commercial SBCs this module uses a light weighted RTOS with minimal latency time and effective use of processor's peripherals. This single board computer has the same set of the serial I/O interfaces as extension modules from fig.5, which provides the same opportunities for communication and remote configuration of the synchronization system. For compactness and lowering the price this module does not support any parallel bus for extension modules. This module will be used for emulations of various signals and for testing of the synchronization system. Processor-FPGA combination allows using this module as a multipurpose component in different systems. For instance this module is used as a timing signal decoder and simulator in some beam diagnostic subsystems in GSI.

The latest device developed for synchronization system is the module based on the 8-bit microprocessor. This module is shown on Fig. 7. The module is equipped by two RS485 and RS 232 interfaces for configuration and one RS485(GSI MIL_STD Bus) interface for STB input. This module is used only for service modules for the synchronization system. At the moment four similar modules are made.

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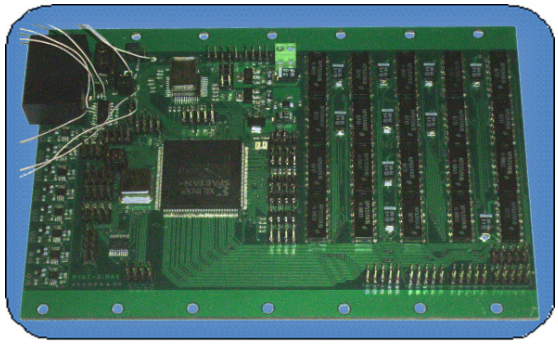

Figure 7. Synchronization module based on Mega microcontroller.

The software developed for this module allows using it as the a service module of the synchronization system. The microprogram loaded into FPGA provides:

- Periodical generation of starting impulses with programmable period from 20mks to 85sec.
- Four inputs for external starting impulses.
- Four inputs for external frequency.
- Twenty 32bit LTG
- Forty FG with programmable pulse duration of the output impulse and light indication.

CONCLUSION

For the moment, a several different modules are designed for synchronization system of TWAC ITEP. These modules allow replacing the existing synchronization system and are ready to be used in future system with new principles of synchronization. Using a single board computer with FPGA allows fast and reliable dynamic reconfiguration of a particular module and the whole synchronization system.

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