

VME BASED DIGITIZERS FOR WAVEFORM MONITORING SYSTEM OF LINEAR INDUCTION ACCELERATOR LIA-20

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Abstract

The Linear Induction Accelerator LIA-20 is being created at the Budker Institute of Nuclear Physics. Waveform monitoring system (WMS) is an important part of LIA-20 control system. WMS includes "slow" and "fast" monitoring subsystems. Three kinds of digitizers have been developed for WMS.

"Slow" subsystem is based on ADCx32. This digitizer uses four 8-channel multiplexed SAR ADCs (8 μ s conversion cycle) with 12 bit resolution. Main feature of this module is program configurable channel sequencing, which allows to measure signals with different timing characteristics.

Two types of digitizers are involved in "fast" subsystem. The first one, ADC4x250-4CH, is 4-channel 250 MSPS digitizer. The second one, ADC4x250-1CH, is single channel digitizer with sample rate of 1 GSPS. Resolution of both devices is 12 bit. "Fast" modules are based on the common hardware.

This paper describes hardware and software architecture of these modules.

INTRODUCTION

The linear induction accelerator with energy of 20 MeV (LIA-20) intended for pulsed X-ray radiography with high space resolution is under development in the BINP (Novosibirsk, Russia). In the total control system one of the most important is the waveform monitoring system. For linear induction accelerators which are high-power, high-voltage pulsed installations, waveform monitoring, i.e. registration of waveforms of signals received from a wide range of sensors in each operating cycle, is the most informative, although very expensive way to control the normal operation of equipment [1, 2].

It is assumed that in the final version the WMS will enable the registration of two thousand waveforms with different durations. Analysis of the data obtained immediately at the end of the operating cycle will make a conclusion about the current condition of the installation elements and their operation in the last cycle. At the same time, data archiving, performed for many operating cycles, and their appropriate processing will allow to identify and study in detail trends in the equipment, the evolution of their parameters and thus to predict possible failures.

Operating cycle of the LIA-20 can be divided into three phases: a preparatory, acceleration phase and an experimental phase. The typical duration of the processes in the preparatory phase are in the range of 0.2 – 20 ms, in the acceleration phase – 100 – 400 ns, and in the experimental phase, when the beam is directed into

several routes, the signal durations are 20 – 50 ns. The signal bandwidth in the first phase does not exceed 10 – 20 kHz, in the second it is 30 – 40 MHz, and in the third – 200 MHz.

Thus, three types of modules are required for arranging the waveform monitoring. The first one is to have the sampling rate 50 – 100 kSPS and can be built based on the multiplexed ADC chips. The second one must provide the sampling rate of 3 – 5 ns/sample. The fastest module should have a speed not less than 1 ns/sample. Note that for a full-scale waveform monitoring is necessary to record signals for the first phase in 1563 channels, for the second – in 840 channels and for the third – in 18 channels.

The following describes structural schemes of modules used in the WMS, discusses the features of the chosen solutions, ways of errors minimizing. Some details of schemes and the resulting device parameters are presented.

SLOW WMS DIGITIZERS ADCX32

"Slow" WMS subsystem provides data acquisition of Pulsed HV System (PHVS) signals (see Fig. 1). PHVS includes 27 HV chargers, 480 pulse modulators with Pulse Forming Networks (PFN) for supplying accelerating inductors, 64 pulsed demagnetizer and 32 magnetic lens supply units. Such parameters as HV charger voltage, PFN voltage, demagnetizer current and magnetic lens current should be measured with an error not exceeding 0.1%. The durations of PHVS elements processes differ significantly as shown in timing diagram of PHVS operation (see Fig. 1). Thus, "slow" WMS should be able to digitize 1563 signals in time range 500 μ s – 20 ms.

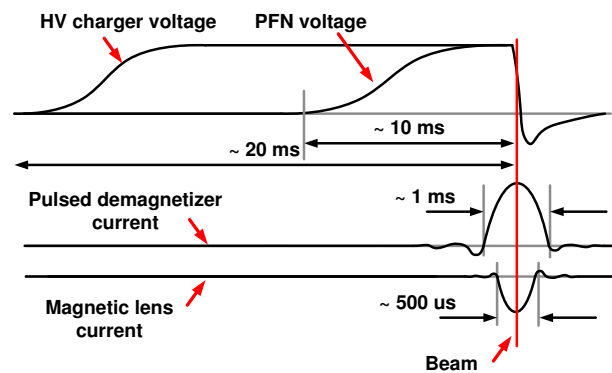


Figure 1: PHVS timing diagram.

The basic idea of "slow" WMS digitizer design is using four 8-channel multiplexed 1 MSPS SAR ADCs with

programmable channel sequencing. Channel sequence configuration determines sampling rate for each ADC channel individually. That allows sampling channels with shorter time duration faster than channels with longer time duration. This approach is illustrated in Fig. 2. Sequence example is shown in timing diagram for the case, when CH.0 of ADC records fast process with twice higher sampling rate than CH.1 and CH.2.

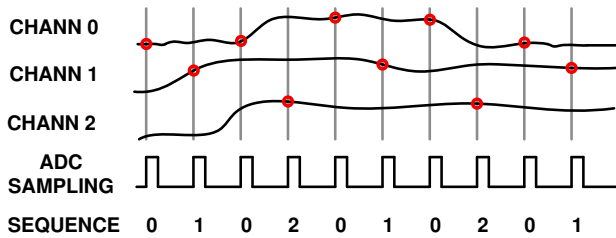


Figure 2: ADC channel sequencing.

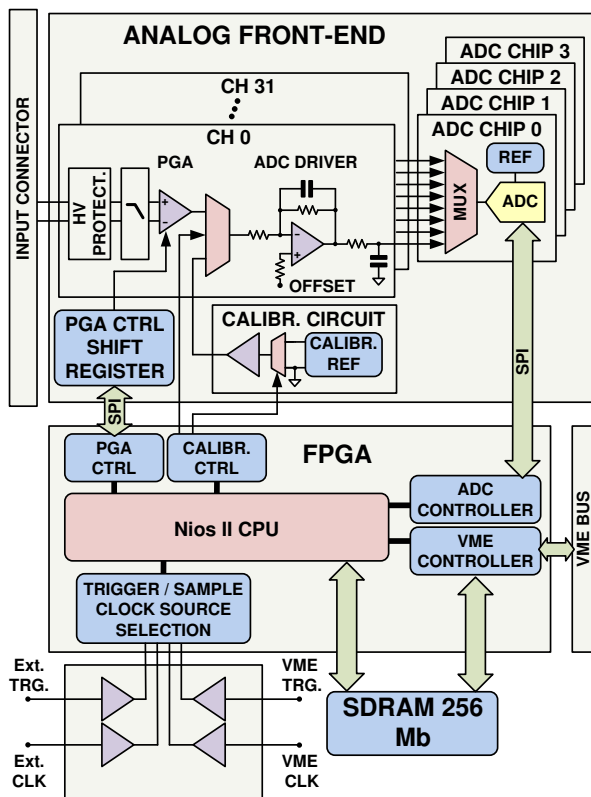


Figure 3: ADCx32 block diagram.

ADCx32 is 32-channel VME digitizer based on channel sequencing technique designed for "slow" WMS subsystem. ADCx32 block diagram is shown in Fig. 3. Core of the digitizer is Nios II embedded CPU implemented in a Cyclone III (Altera FPGA). Core provides VME interface support, driving of SDRAM memory, trigger and sample clock sources selection and analog front-end control. Front-end is built on four ADC chips and 32 input channels circuits. Digitizer inputs equipped with HV protection (100 V), 50 kHz filtering and PGAs. See Table 1 for ADCx32 specifications.

Necessary precision was achieved by using calibration procedure, which includes measurements of zero and scale errors of drivers and ADCs and applying built-in data correction algorithm.

Table 1: ADCx32 Specifications

Sampling rate	1 MSPS (max)
Bandwidth, -3dB	50 kHz
Ranges	±1 V, ±2 V, ±4 V, ±8 V
Resolution	12 bit
Absolute error	± 3*10 ⁻⁴ FS
Total noise (RMS)	< 0.7 LSB
SNR	75.3 dB _{FS} in the operating band
Buffer size	524 288 samples per channel

FAST DIGITIZERS FAMILY ADC4X250

A relatively small number of signals recorded in the third phase, makes uneconomical the development of the device with 1 GSPS sample rate, if take into account labour expenditures. On the other hand, the purchase of a number of modules, each of which costs about \$ 12,000, not a satisfactory one. However, it is clear that the structural schemes of modules of the second and third types (ADC4x250-4CH, ADC4x250-1CH) are identical and include fast ADCs, buffer memory, accurate synchronization elements and VME interface. In this regard, it looks attractive variant when first developed slower module type, and then based on it is realized the fastest device.

Let us discuss the structural scheme which allows realizing proposed method. It is shown in Fig. 4.

The module consists of an input (replaceable) and common parts. The marked by dashed part of the structure in the figures is a uniform hardware platform. This part remains unchanged for both modules and contains four 250 MSPS 12-bit ADCs with their drivers, synchronization and timing circuit as well as digital equipment. These parts implemented as a separate PCBs and stacked with each other by mezzanine way.

It the case of four-channel device (ADC4x250-4CH) replacement part consists of four input amplifiers. Each amplifier corresponds to one channel. In this case all ADCs are driven by synchronous clocks. Therefore, the sample rate of such device coincides with the sample rate of one ADC and equals 250 MSPS. The bandwidth of the ADC4x250-4CH is determined by the input amplifiers and ADC and equals 75 MHz.

One-channel device is obtained by replacing the input amplifier and program reconfiguration of a clock circuit. To increase the high sample rate of A/D conversion it is needed to drive ADCs by clock signals with a phase shift of 90° (Fig. 5). ADCs work sequentially in time. Therefore, sample rate for one input is quadrupled and eventually equals 1000 MSPS.

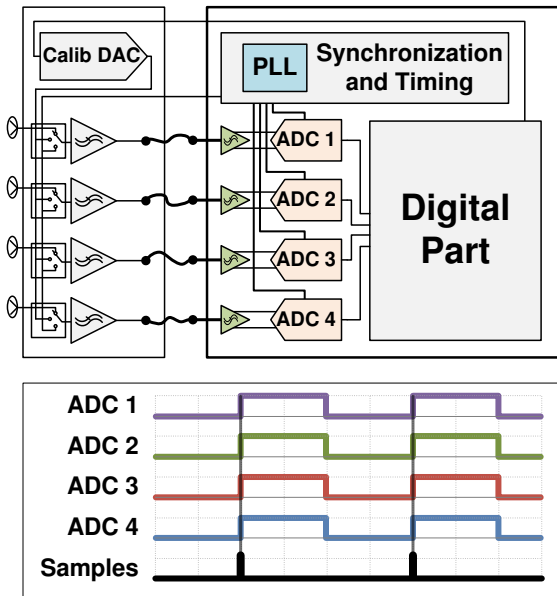


Figure 4: The structure of ADC4x250-4CH and its clock sequence.

Following this way, two-channel device with 500 MSPS may be easily made if it will be needed.

The advantages of this approach are the same circuit solutions, unified element base, tracing the multilayer PCB. It is important to say that LIA-20 control system including WMS using of VME64x standard with advanced extensions that providing inter-module synchronization in VME crate [3]. A necessary of supporting this quite complex interface and the need to develop devices that provide such synchronization are additional reasons for creating uniform hardware platform.

Of course, the proposed approach has the additional charges, which require more complex "firmware" for PLDs, additional calibration procedures and specific

Table 2: ADC4x250 Family Specifications

	ADC4x250-4CH	ADC4x250-1CH
Sample rate	250 MSPS	1000 MSPS
Bandwidth, -3dB	75 MHz	300 MHz
Voltage ranges	±0.5 V, ±1 V, ±2 V, ±4 V	
Resolution	12 bit	
Buffer length	786 432 samples/ch	3 145 728 samples/ch
Static noise (RMS)	< 0.8 LSB	< 1 LSB
Phase noise (RMS)	< 0.7 ps	< 0.7 ps
Crosstalk @ 50 MHz	< -60 dB	—
SNR	62.7 dB _{FS} @ 11 MHz	62 dB _{FS} @ 110 MHz
SINAD	61.8 dB _{FS} @ 11 MHz	45.6 dB _{FS} @ 110 MHz

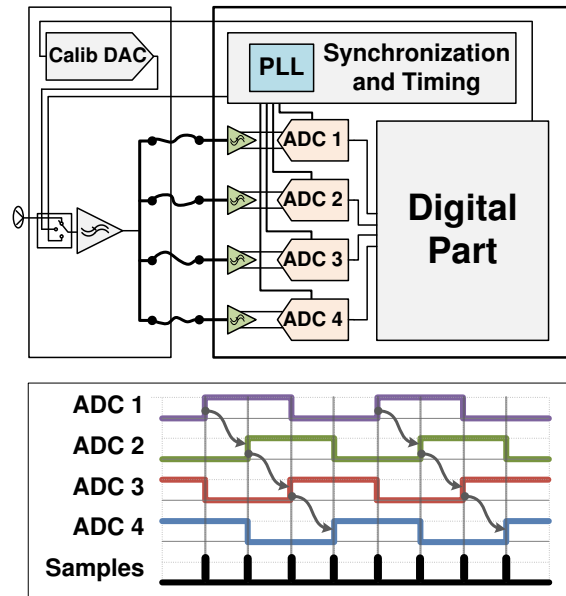


Figure 5: The structure of ADC4x250-1CH and its clock sequence.

signal processing. For one-channel device in addition to standard static (zero and scale) calibration, dynamic calibration are implemented which allow to measure difference of channels delays. A number of signal correction methods based on dynamic calibration are added as part of signal processing.

Characteristics of the ADC4x250 family digitizers are specified in Table 2.

CONCLUSION

Three kinds of VME-based waveform digitizers have been developed. These modules are intended for creating Waveform Monitoring System of the Linear Induction Accelerator LIA-20, but can be used in other VME-based systems to arrange multichannel recording signals in wide time range.

A pilot batch of modules is produced and tested in real experiments. Currently it is prepared serial production of all three models of digitizers.

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